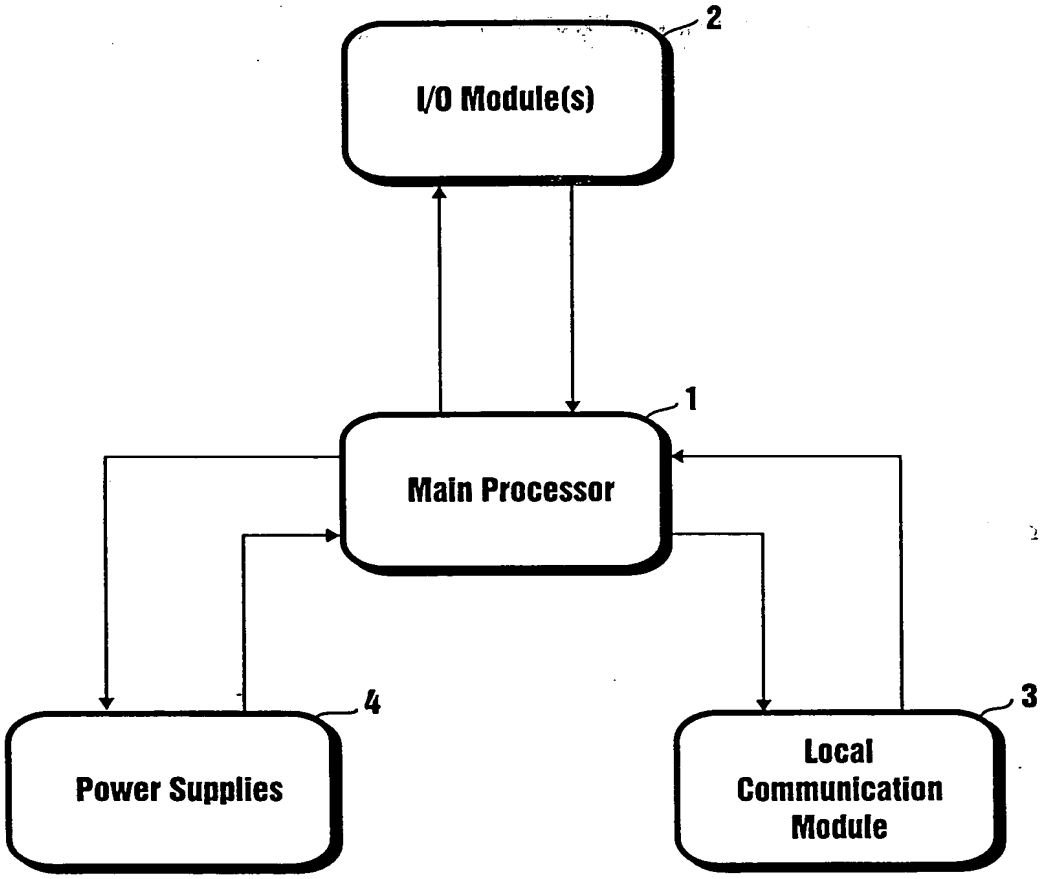
2
I/O Module(s)
1
Main Processor
4
Power Supplies
3
Local
Communication
Module

Figure 1

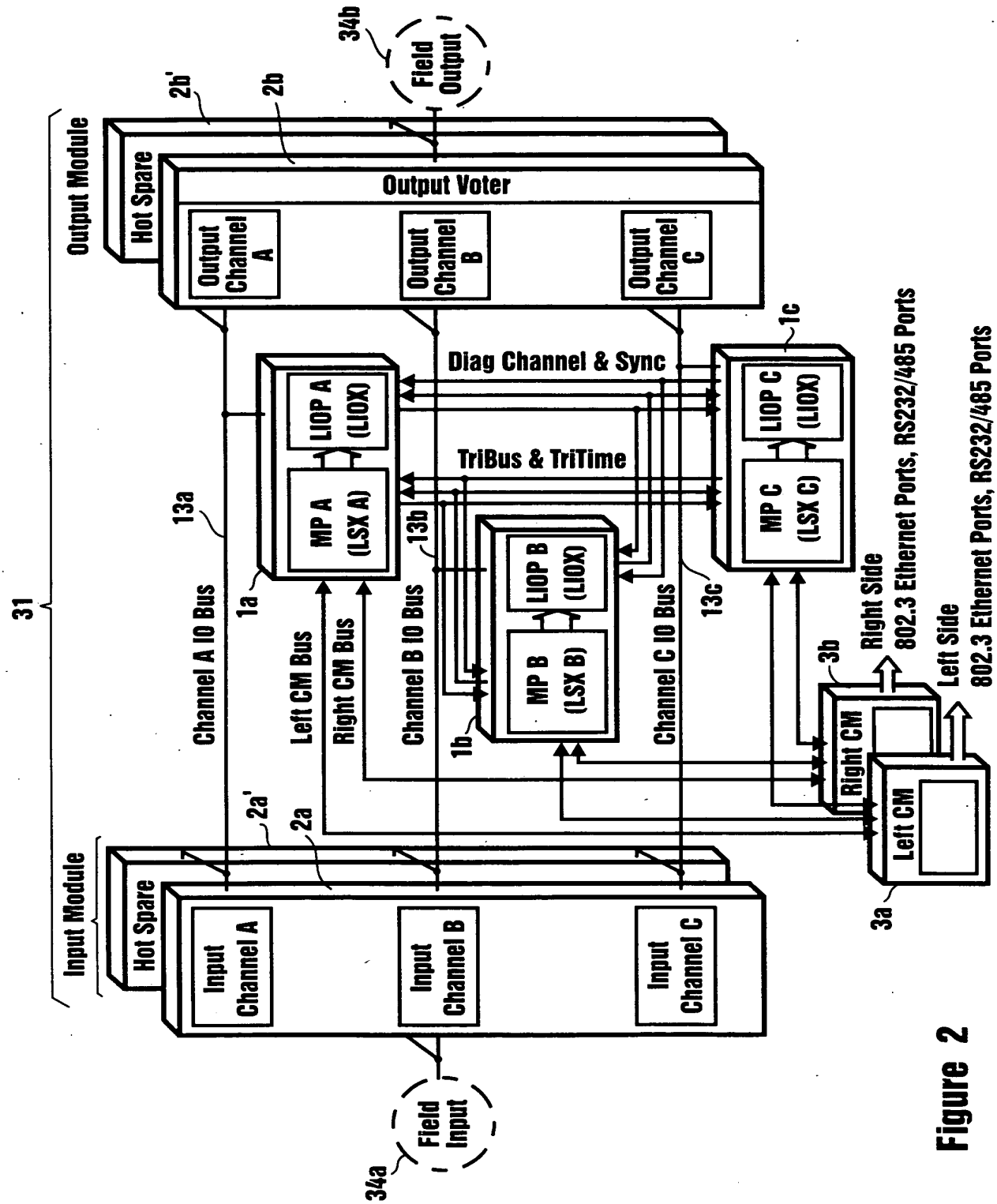
31
Output Module
Hot Spare
Output Voter
Output Channel A
Output Channel B
Output Channel C
2b'
2b
34b
Field Output
Diag Channel & Sync
TriBus & TriTime
LIOP A (LIOX)
MP A (LSX A)
LIOP B (LIOX)
MP B (LSX B)
LIOP C (LIOX)
MP C (LSX C)
1a
1b
1c
13a
13b
13c
Channel A IO Bus
Channel B IO Bus
Channel C IO Bus
Left CM Bus
Right CM Bus
Right CM
Left CM
3a
3b
Right Side
802.3 Ethernet Ports, RS232/485 Ports
Left Side
802.3 Ethernet Ports, RS232/485 Ports
Input Module
Hot Spare
Input Channel A
Input Channel B
Input Channel C
2a'
2a
34a
Field Input

Figure 2

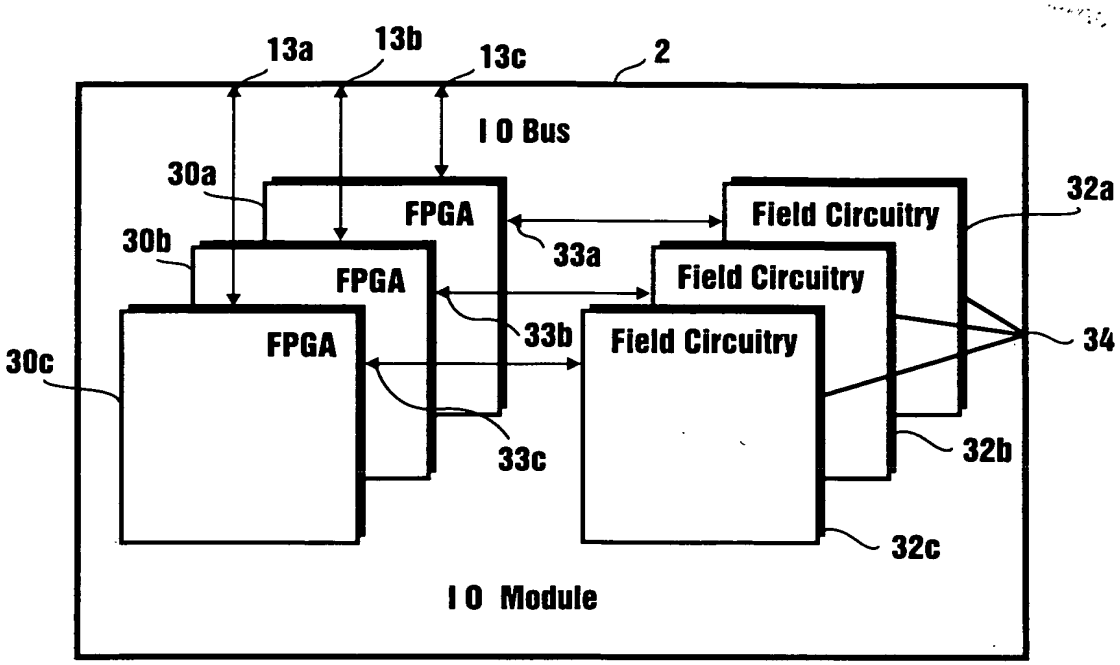

Figure 3

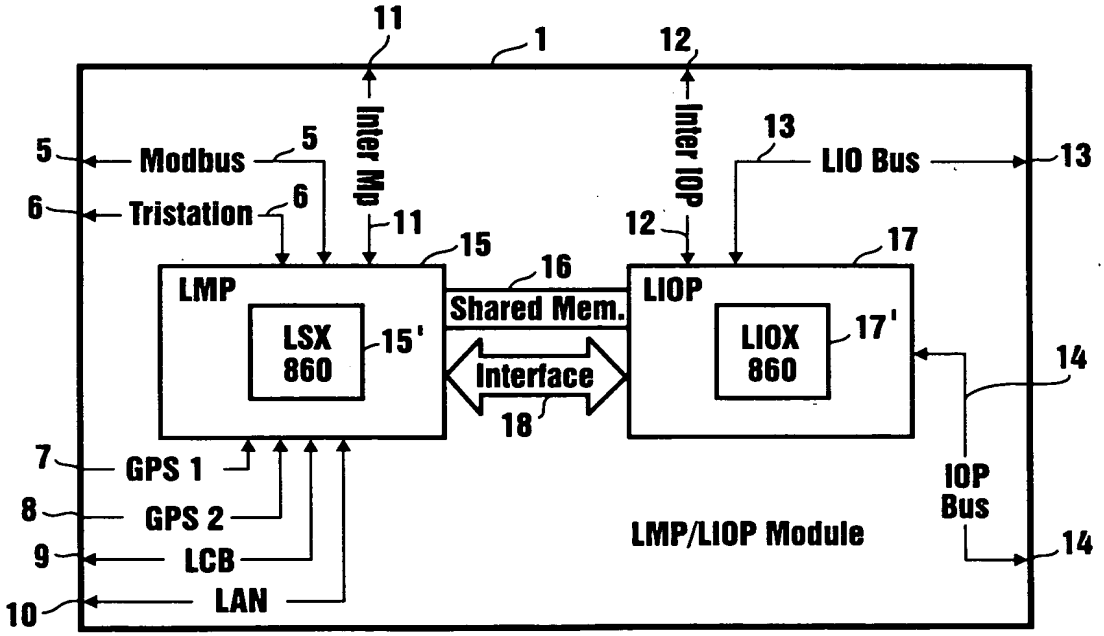

Figure 4

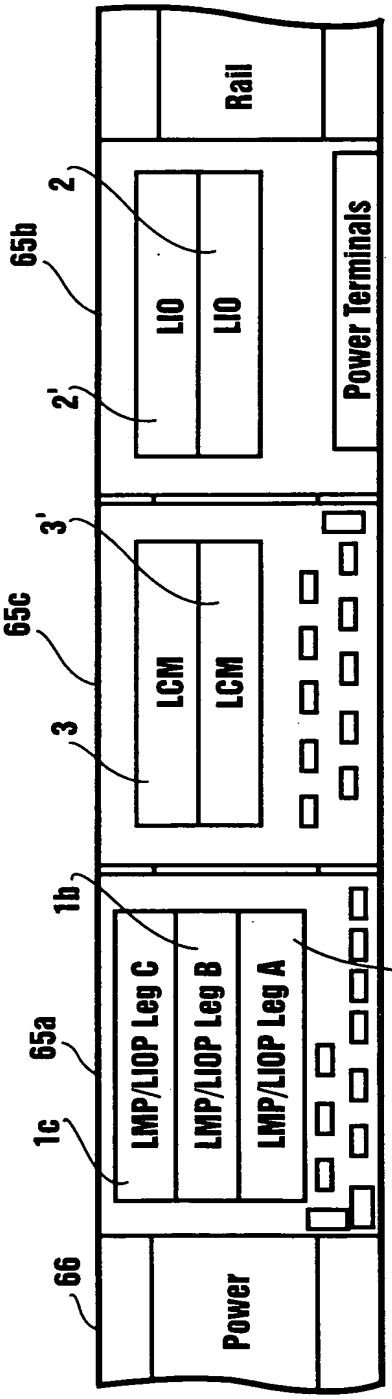

Figure 5B

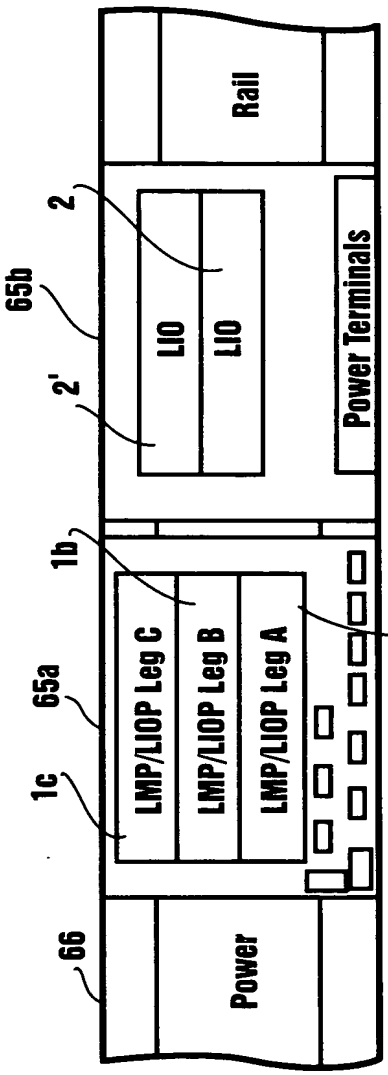

Figure 5A

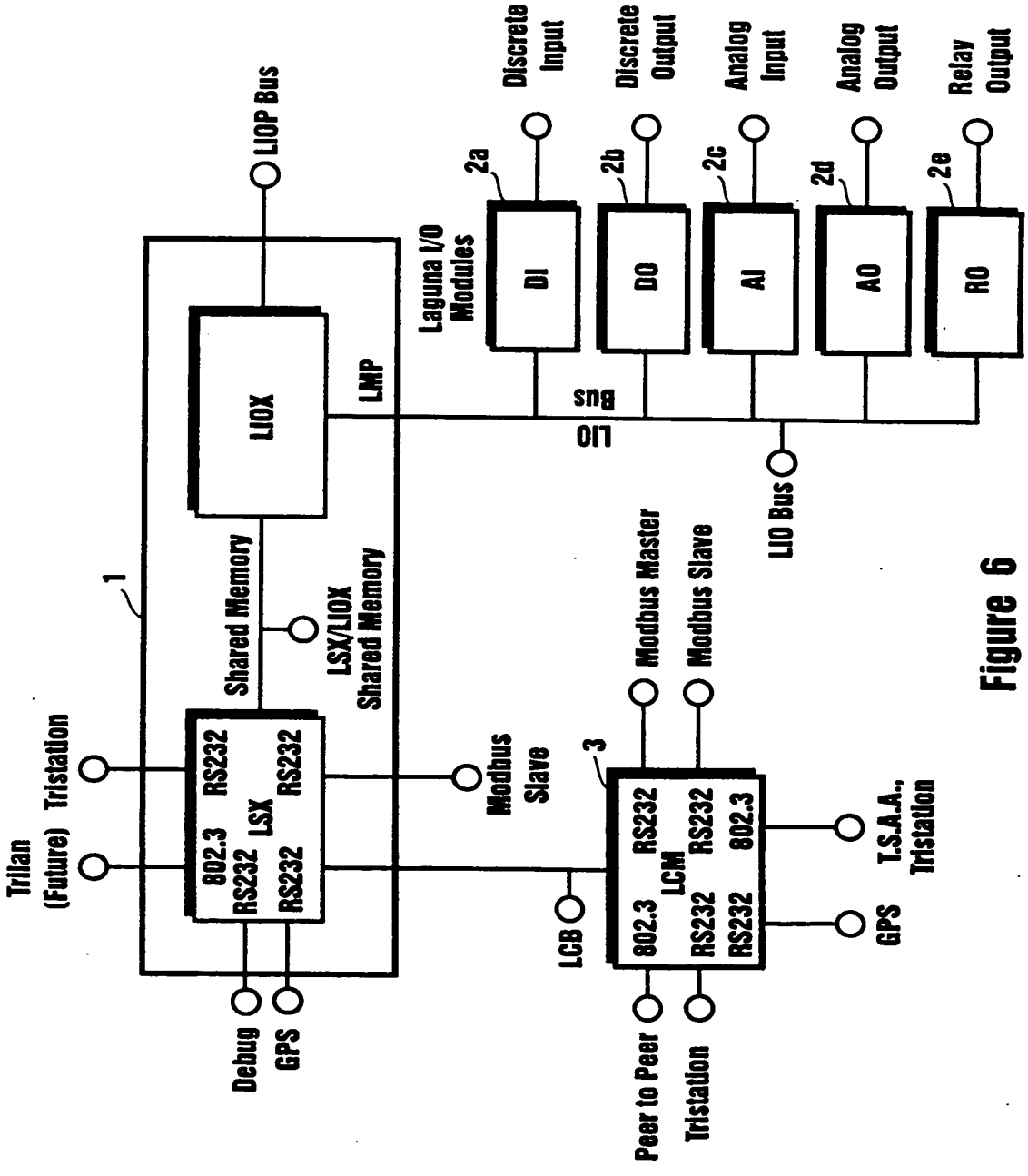
Discrete Input
Discrete Output
Analog Input
Analog Output
Relay Output
2a
2b
2c
2d
2e
Laguna I/O Modules
DI
DO
AI
AO
RO
LIOP Bus
LIOX
LMP
LIO Bus
LIO Bus
1
Shared Memory
LSX/LIOX Shared Memory
Trilan (Future)
Tristation
802.3
RS232
LSX
RS232
RS232
RS232
Modbus Slave
Modbus Master
Modbus Slave
3
LCB
802.3
RS232
LCM
RS232
802.3
RS232
RS232
T.S.A.A., Tristation
GPS
Peer to Peer
Tristation
Debug
GPS

Figure 6

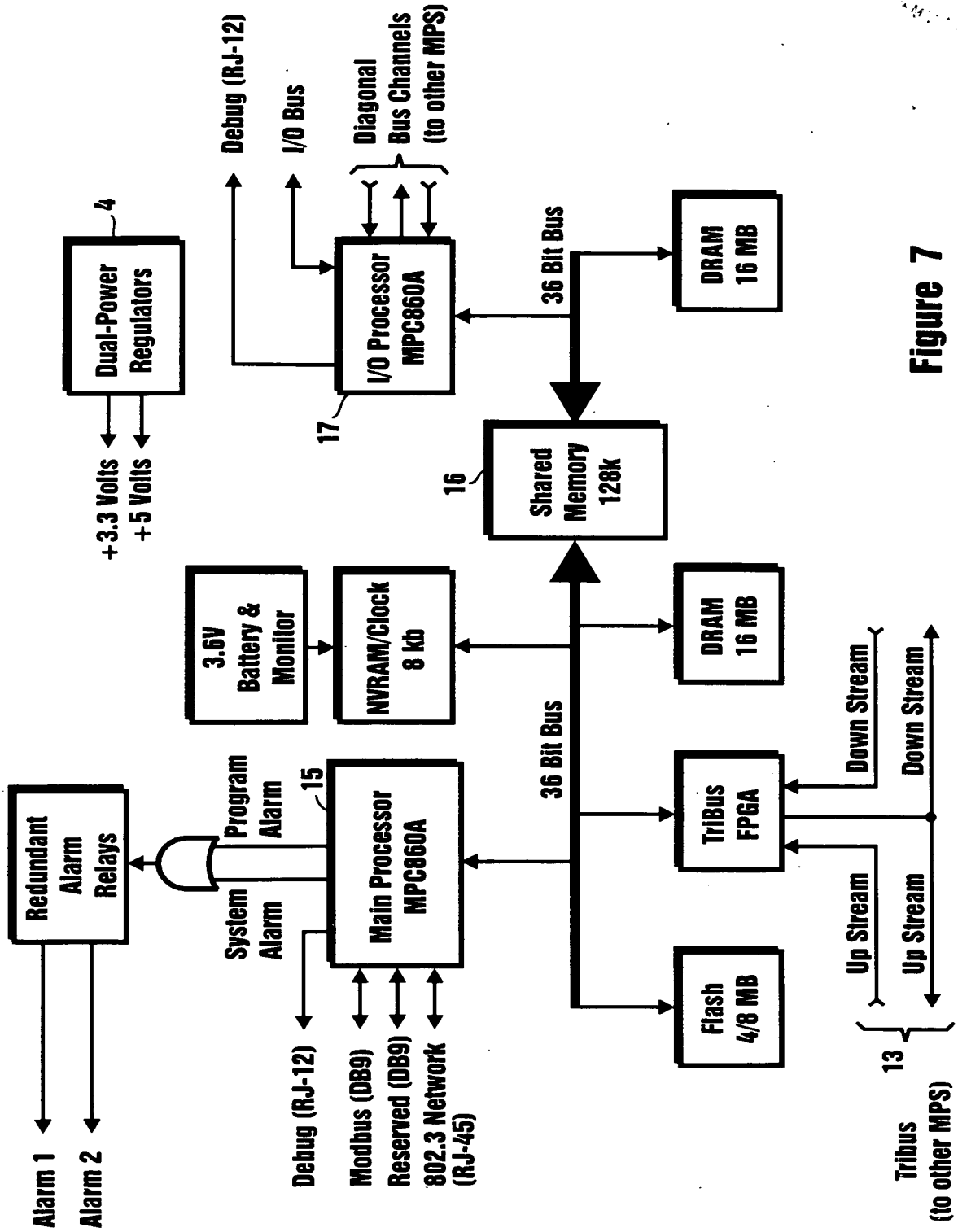
Debug (RJ-12)
I/O Bus
Diagonal Bus Channels (to other MPS)
4
Dual-Power Regulators
+3.3 Volts
+5 Volts
I/O Processor MPC860A
17
36 Bit Bus
DRAM 16 MB
16
Shared Memory 128k
3.6V Battery & Monitor
NVRAM/Clock 8 kb
DRAM 16 MB
Down Stream
Down Stream
Redundant Alarm Relays
Program Alarm
15
Main Processor MPC860A
36 Bit Bus
TriBus FPGA
Alarm 1
Alarm 2
System Alarm
Debug (RJ-12)
Modbus (DB9)
Reserved (DB9)
802.3 Network (RJ-45)
Flash 4/8 MB
Up Stream
Up Stream
13
Tribus (to other MPS)

Figure 7

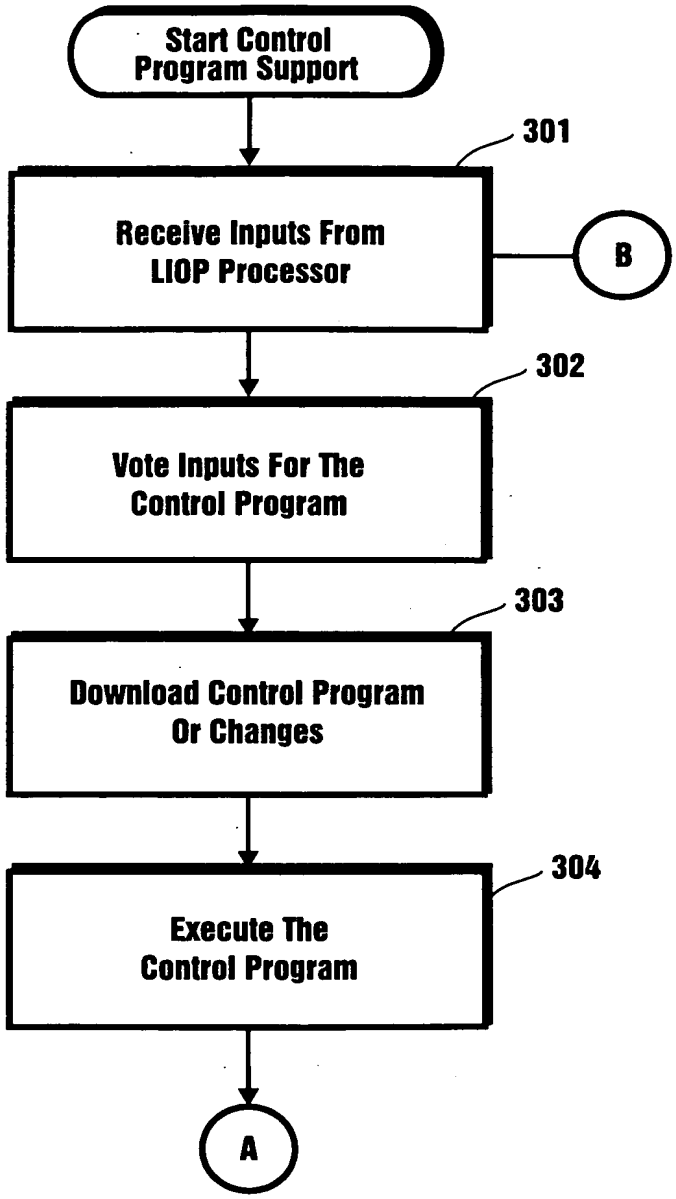
Start Control Program Support
301
Receive Inputs From LIOP Processor
B
302
Vote Inputs For The Control Program
303
Download Control Program Or Changes
304
Execute The Control Program
A

Figure 8A

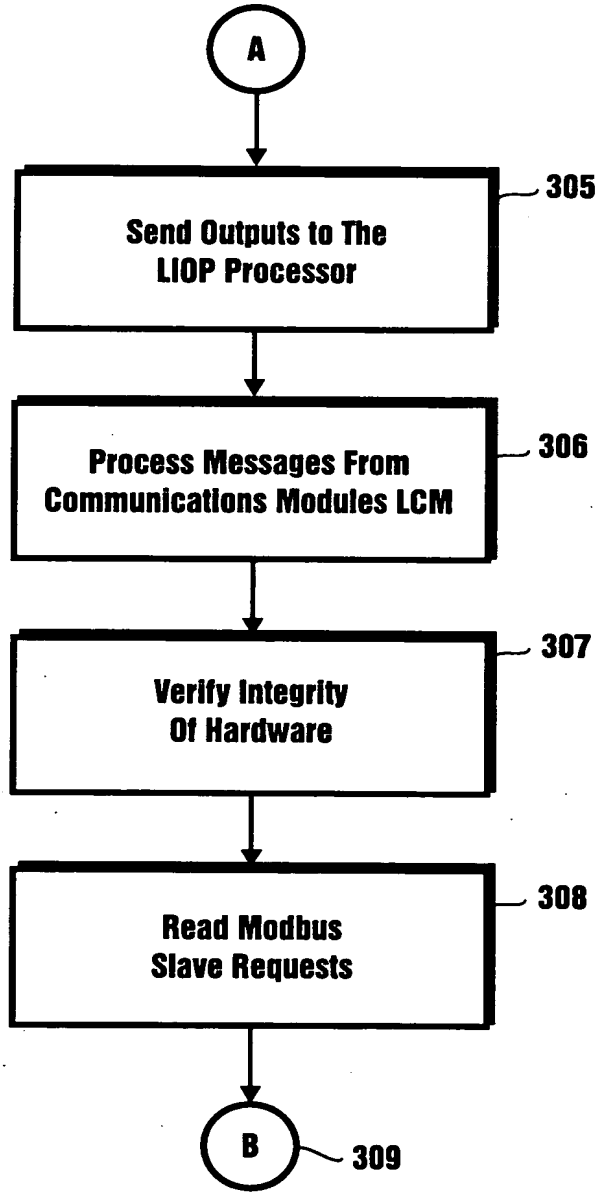
A
Send Outputs to The LIOP Processor
305
Process Messages From Communications Modules LCM
306
Verify Integrity Of Hardware
307
Read Modbus Slave Requests
308
B
309

Figure 8B

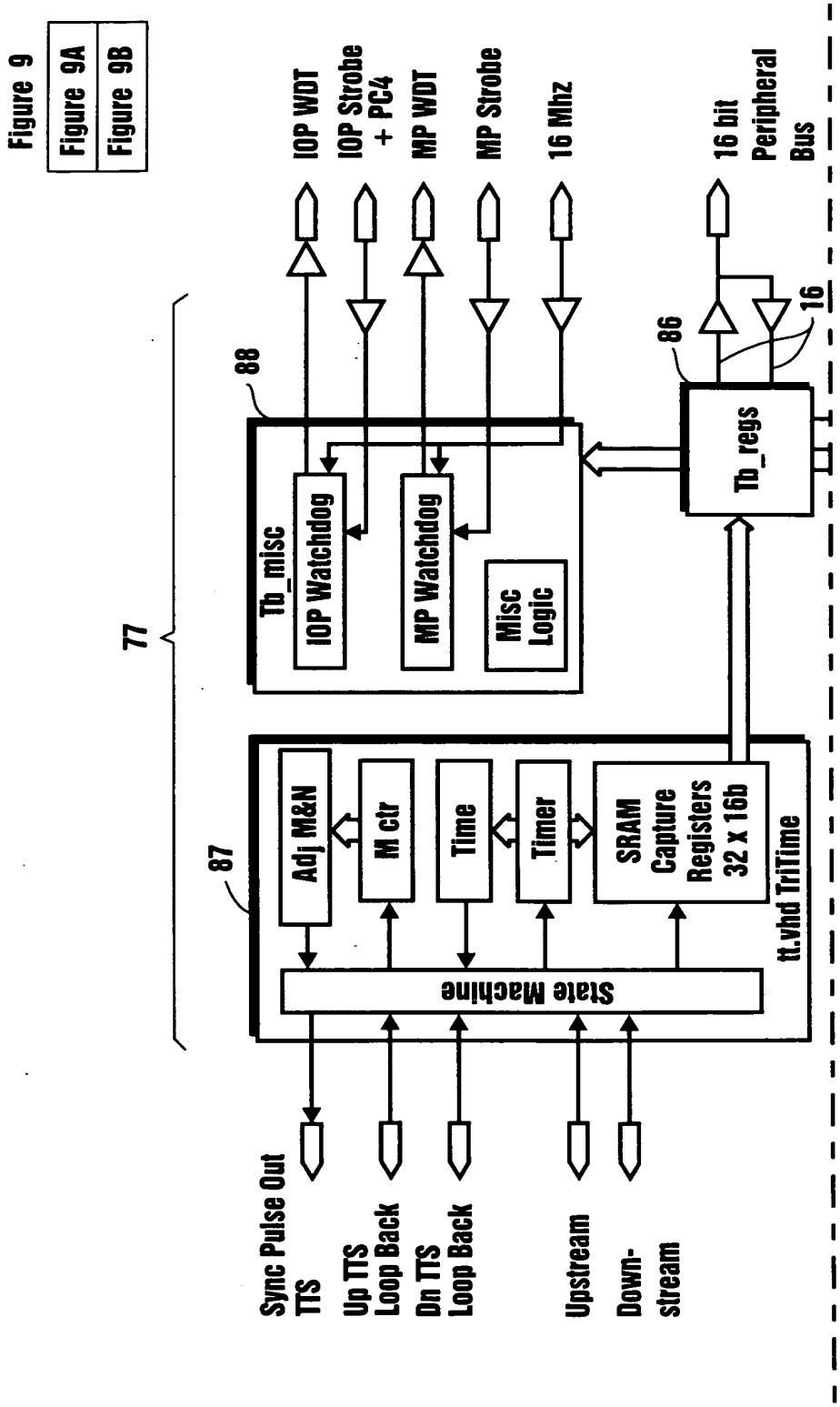
Figure 9
Figure 9A
Figure 9B
77
88
87
86
16
IOP WDT
IOP Strobe + PC4
MP WDT
MP Strobe
16 Mhz
16 bit Peripheral Bus
Tb_misc
IOP Watchdog
MP Watchdog
Misc Logic
Tb_regs
Adj M&N
M ctr
Time
Timer
SRAM Capture Registers 32 x 16b
State Machine
tt.vhd TriTime
Sync Pulse Out TTS
Up TTS Loop Back
Dn TTS Loop Back
Upstream
Down-stream

Figure 9A

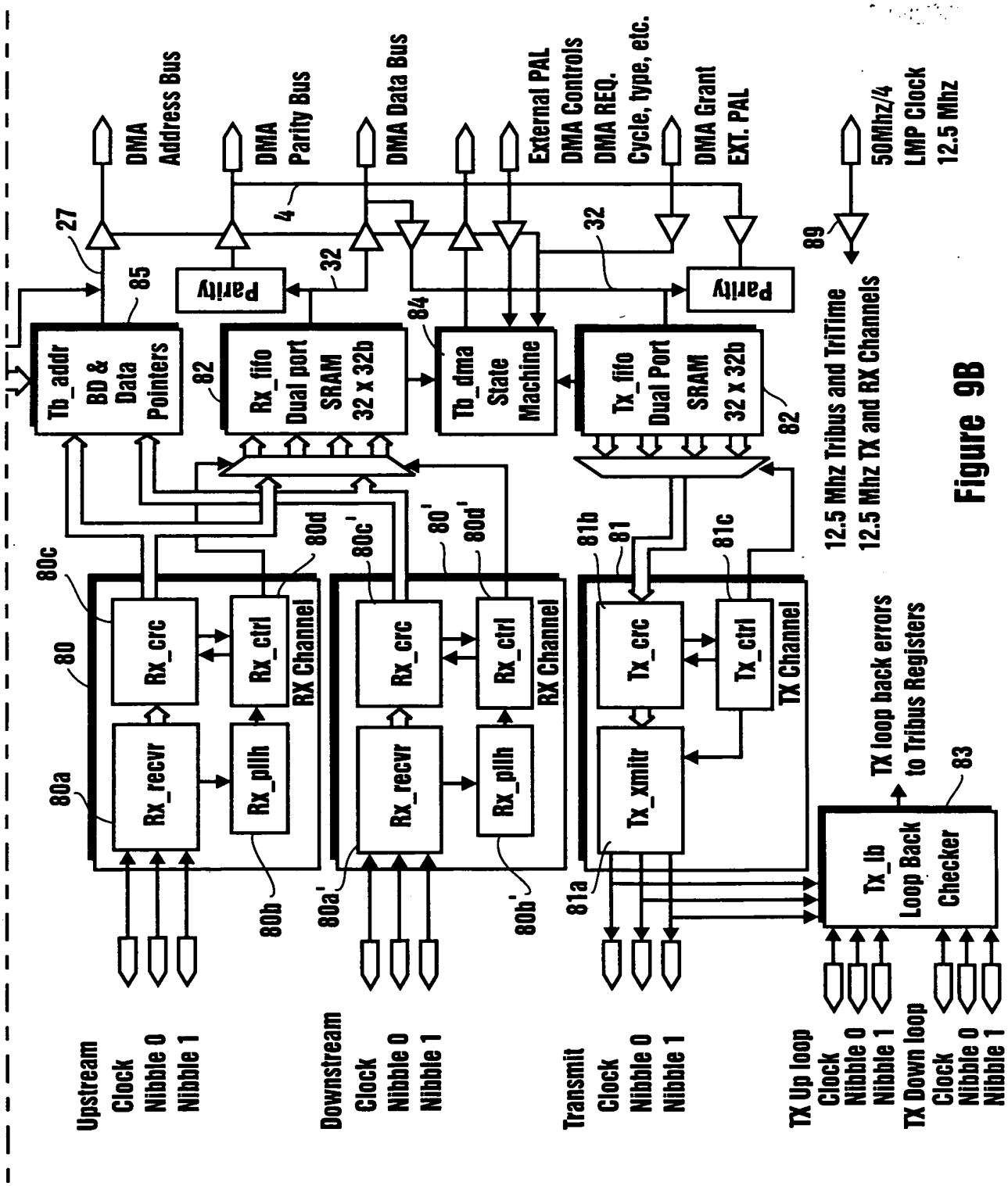
DMA Address Bus
DMA Parity Bus
DMA Data Bus
External PAL DMA Controls DMA REQ. Cycle, type, etc.
DMA Grant EXT. PAL
50Mhz/4 LMP Clock 12.5 Mhz
27
4
32
32
89
85
84
82
82
Parity
Parity
Tb_addr BD & Data Pointers
Rx_fifo Dual port SRAM 32 x 32b
Tb_dma State Machine
Tx_fifo Dual Port SRAM 32 x 32b
12.5 Mhz Tribus and TriTime
12.5 Mhz TX and RX Channels
80
80a
80b
80c
80d
80'
80a'
80b'
80c'
80d'
81a
81b
81
81c
Rx_crc
Rx_ctrl
RX Channel
Rx_recvr
Rx_pilh
Tx_crc
Tx_ctrl
TX Channel
Tx_xmitr
Tx_lb Loop Back Checker
83
TX loop back errors to Tribus Registers
Upstream Clock Nibble 0 Nibble 1
Downstream Clock Nibble 0 Nibble 1
Transmit Clock Nibble 0 Nibble 1
TX Up loop Clock Nibble 0 Nibble 1
TX Down loop Clock Nibble 0 Nibble 1

Figure 9B

09/467669

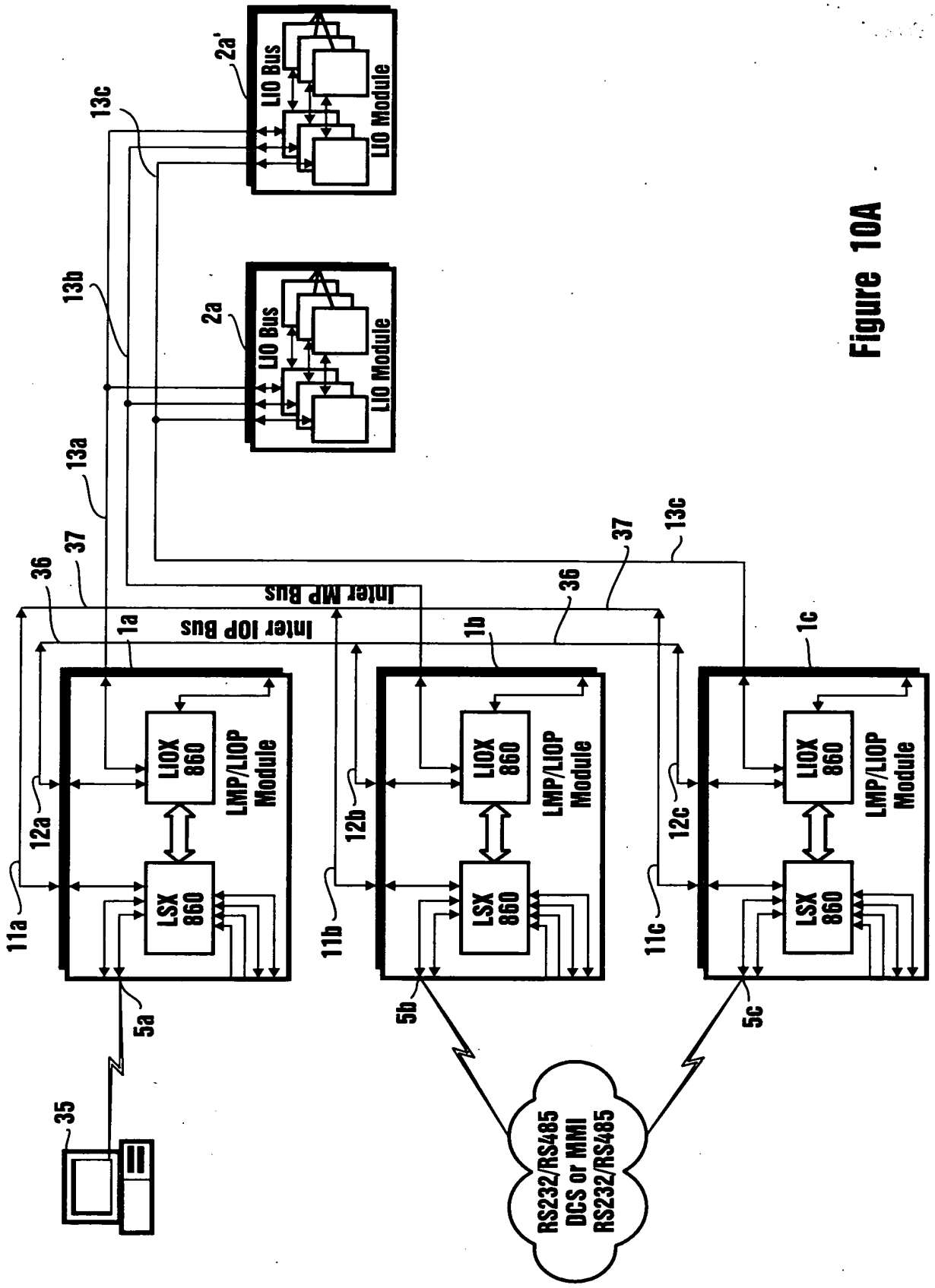

Figure 10A

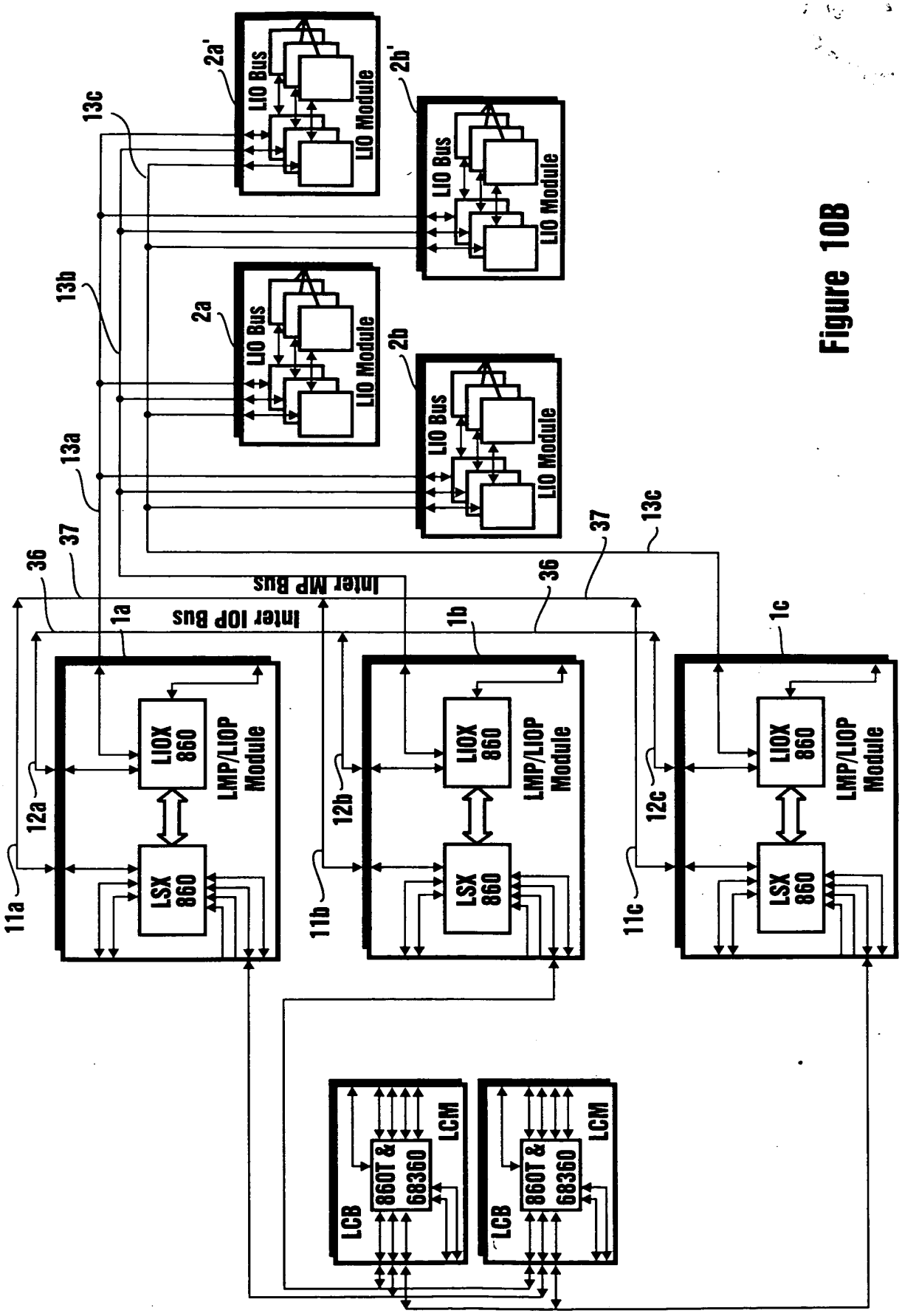
2a'
LIO Bus
LIO Module
2b'
13c
2a
2b
13b
13a
37
36
Inter MP Bus
Inter IOP Bus
1a
1b
1c
LIOX 860
LSX 860
LMP/LIOP Module
12a
12b
12c
11a
11b
11c
LCB
860T & 68360
LCM

Figure 10B

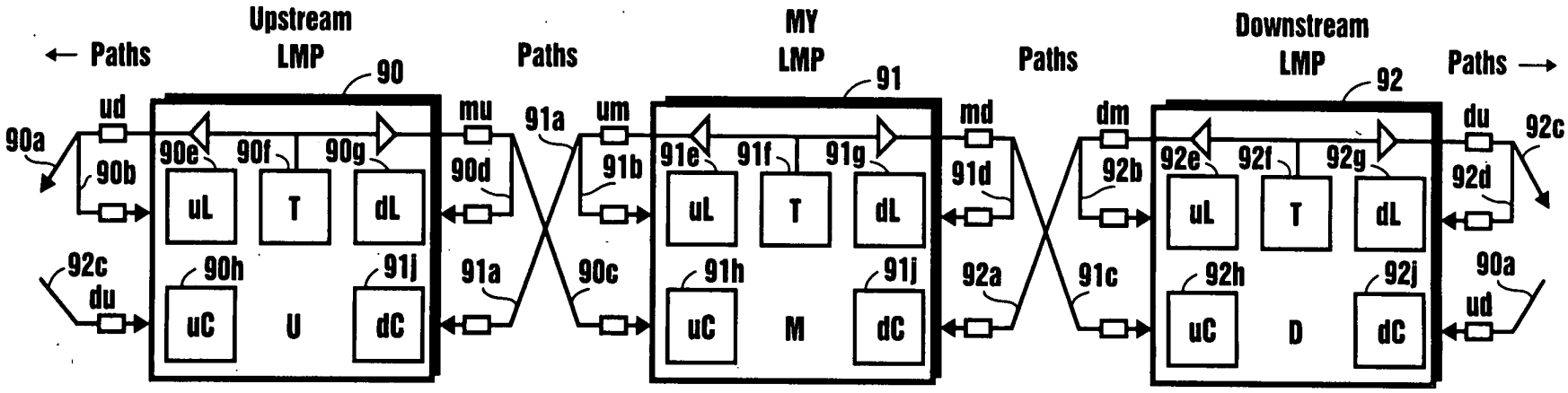

Figure 11A

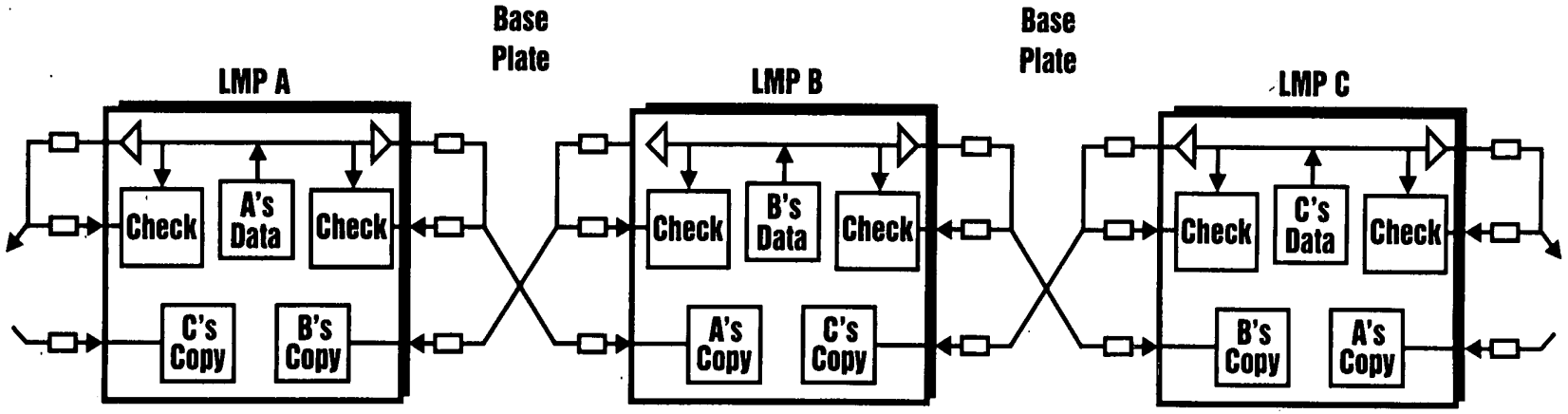

Figure 11B

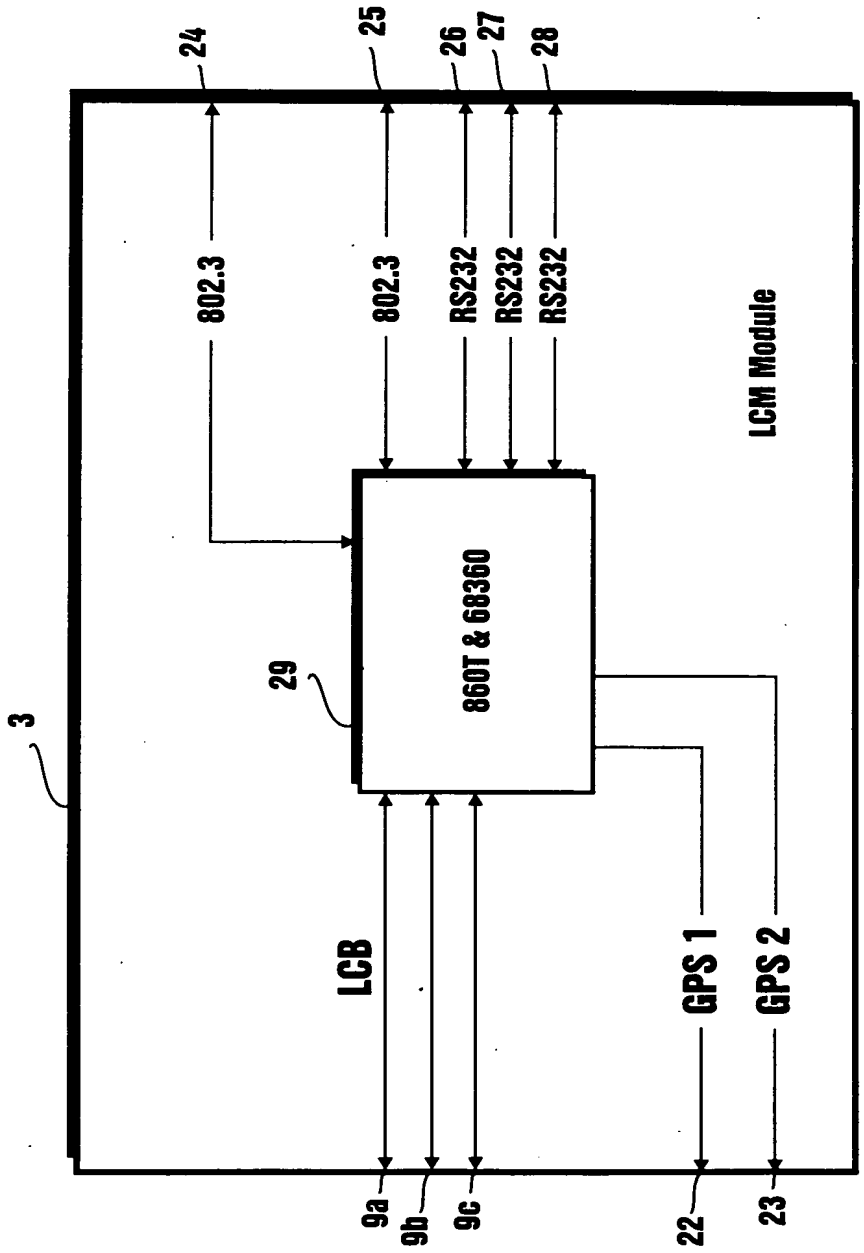
24
25
26
27
28
802.3
802.3
RS232
RS232
RS232
LCM Module
860T & 68360
29
3
LCB
GPS 1
GPS 2
9a
9b
9c
22
23

Figure 12

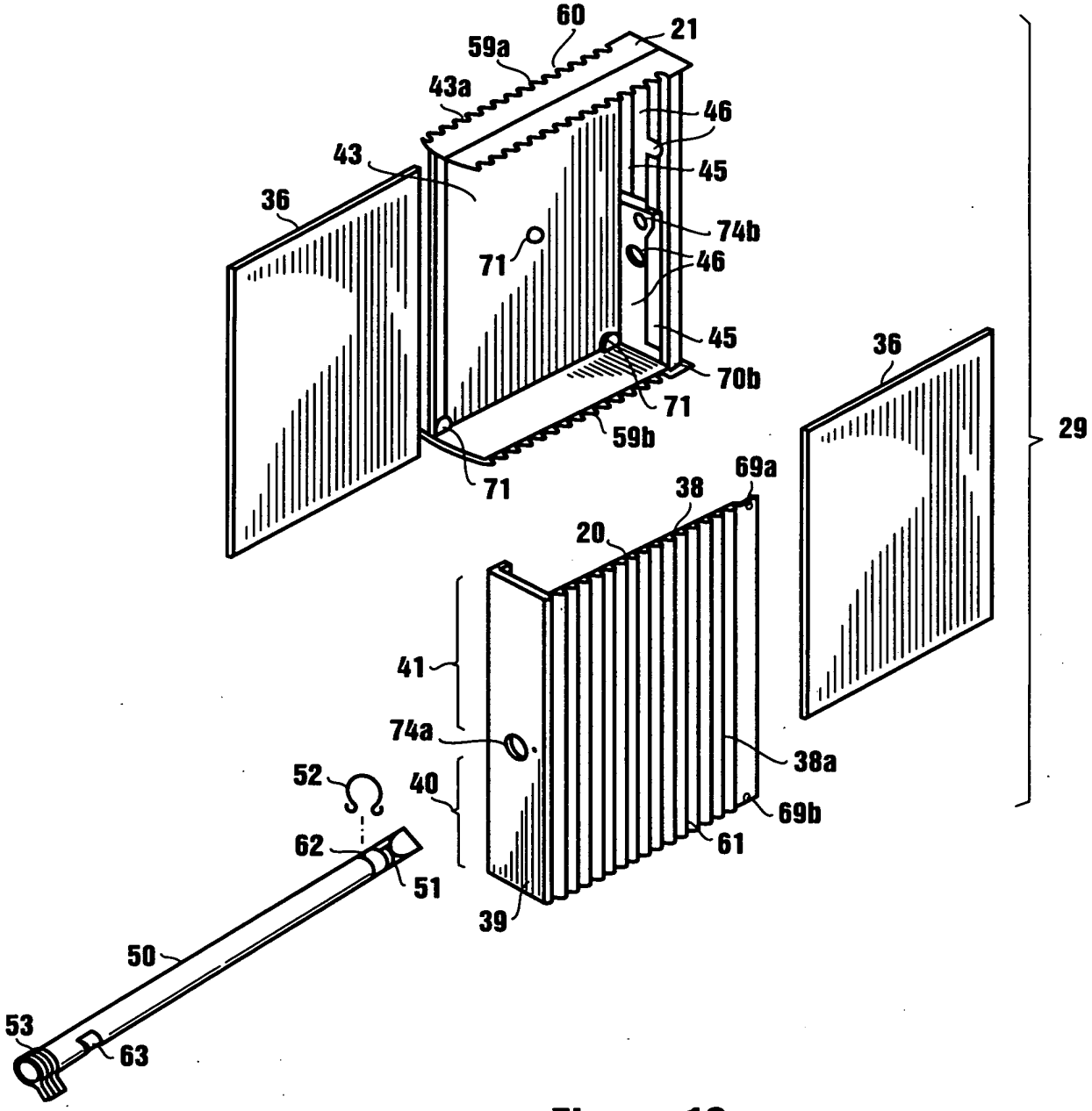
60
21
59a
43a
46
43
45
36
74b
71
46
45
36
70b
71
59b
29
71
69a
38
20
41
74a
38a
52
40
69b
62
61
51
39
50
53
63

Figure 13

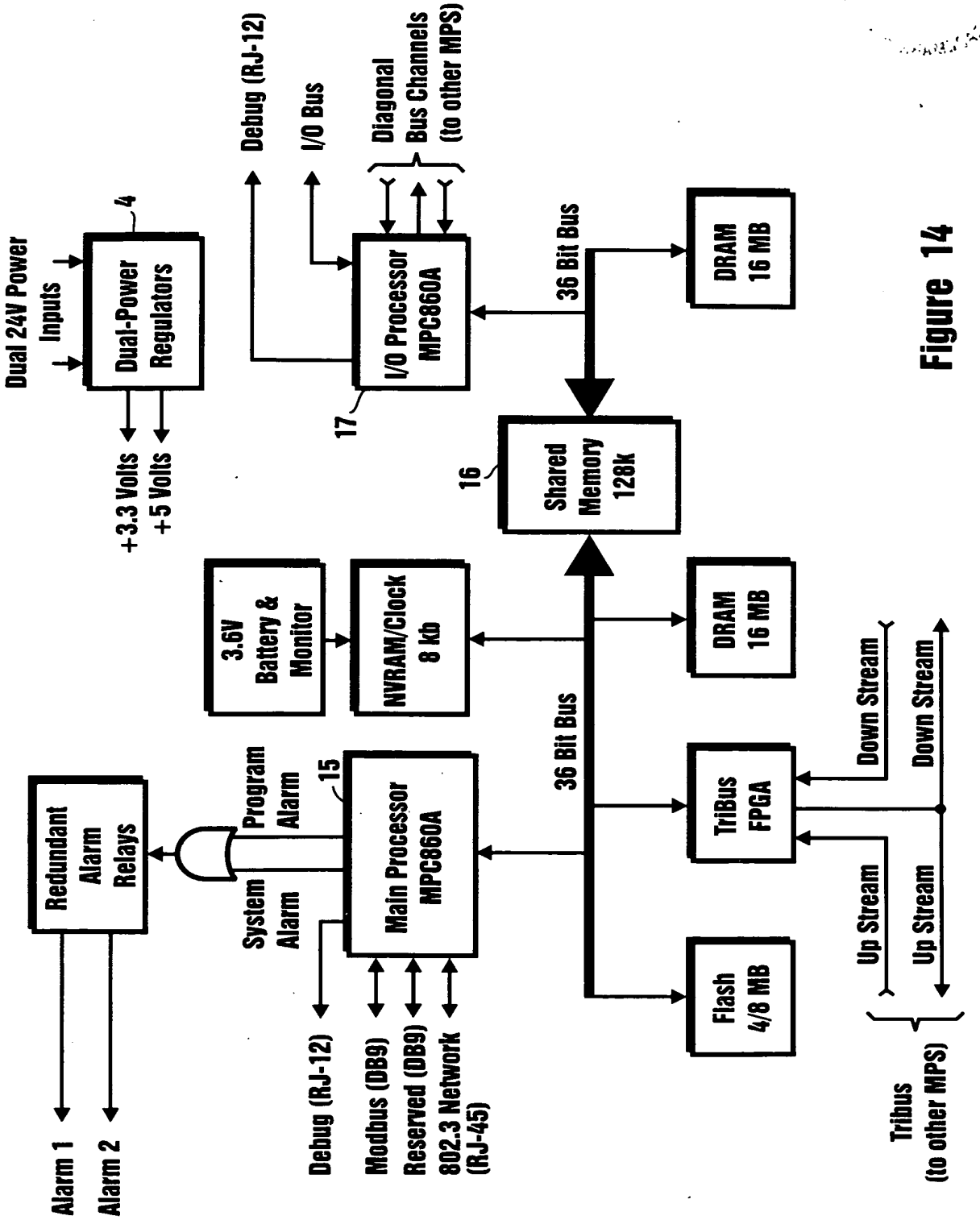
Dual 24V Power Inputs
Dual-Power Regulators
4
+3.3 Volts
+5 Volts
Debug (RJ-12)
I/O Bus
Diagonal Bus Channels (to other MPS)
I/O Processor MPC860A
17
36 Bit Bus
DRAM 16 MB
16
Shared Memory 128k
3.6V Battery & Monitor
NVRAM/Clock 8 kb
DRAM 16 MB
Redundant Alarm Relays
Program Alarm
System Alarm
15
Main Processor MPC860A
36 Bit Bus
TriBus FPGA
Down Stream
Down Stream
Up Stream
Up Stream
Flash 4/8 MB
Alarm 1
Alarm 2
Debug (RJ-12)
Modbus (DB9)
Reserved (DB9)
802.3 Network (RJ-45)
Tribus (to other MPS)

Figure 14

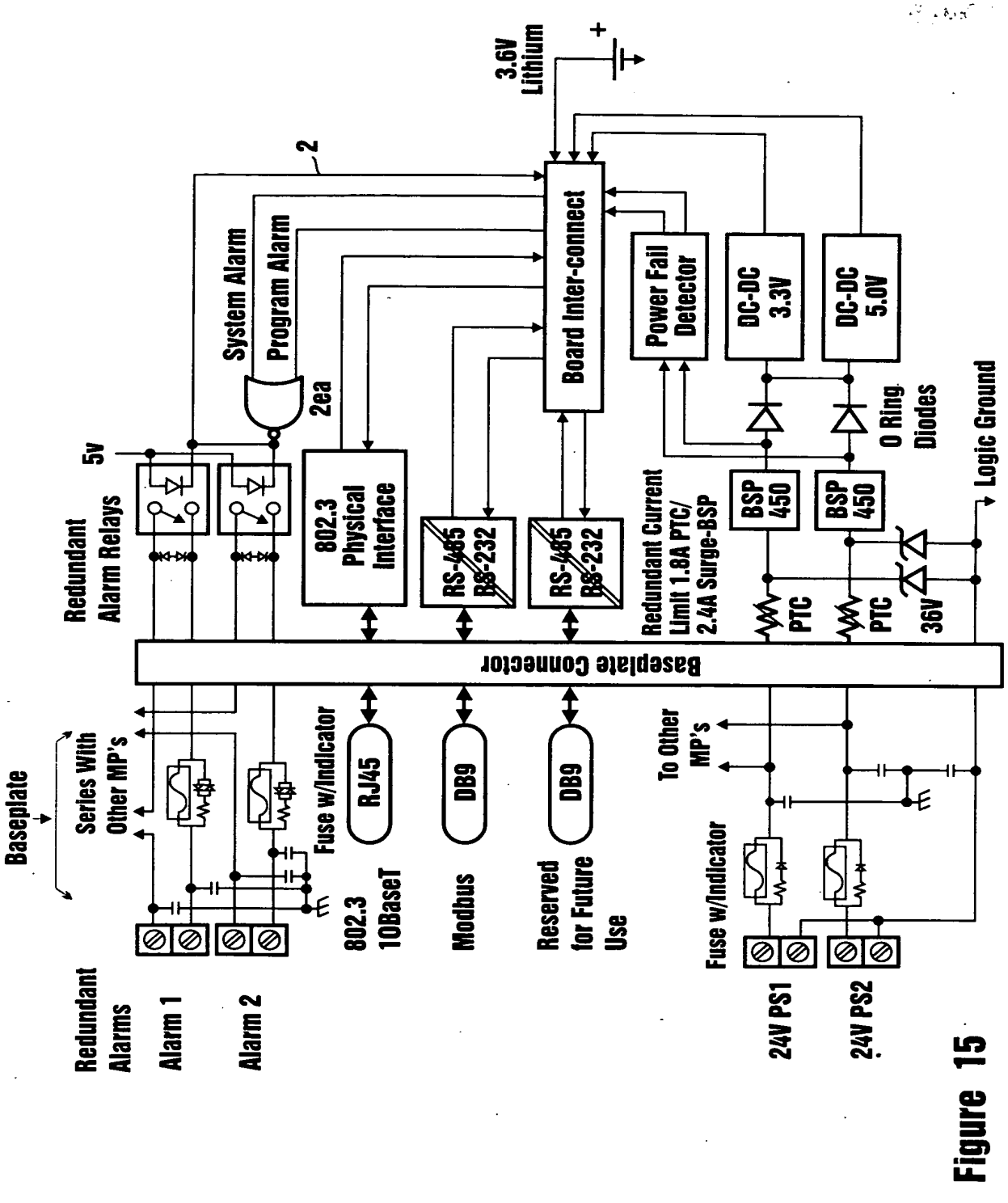
3.6V Lithium
+
2
System Alarm
Program Alarm
2ea
Board Inter-connect
Power Fail Detector
DC-DC 3.3V
DC-DC 5.0V
5v
802.3 Physical Interface
RS-485 RS-232
RS-485 RS-232
Redundant Alarm Relays
Redundant Current Limit 1.8A PTC/ 2.4A Surge-BSP
BSP 450
BSP 450
O Ring Diodes
Logic Ground
PTC
PTC
36V
Baseplate Connector
Baseplate
Series With Other MP's
Fuse w/Indicator
RJ45
DB9
DB9
To Other MP's
802.3 10BaseT
Modbus
Reserved for Future Use
Fuse w/Indicator
Redundant Alarms
Alarm 1
Alarm 2
24V PS1
24V PS2

Figure 15

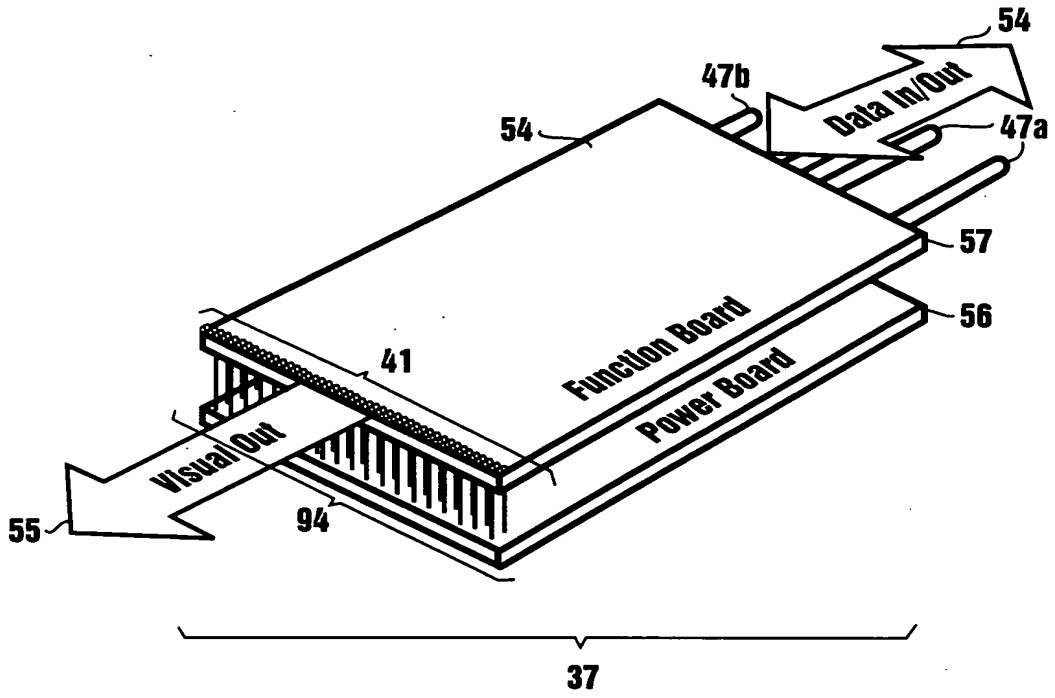

Figure 16

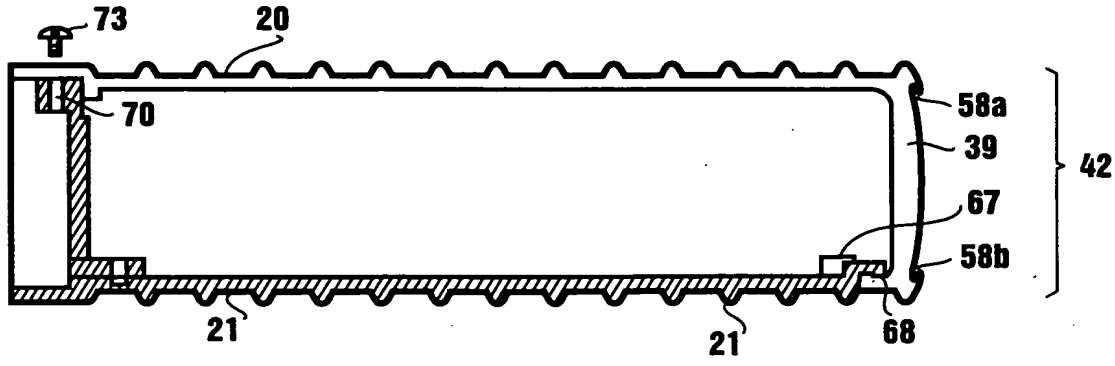

Figure 17

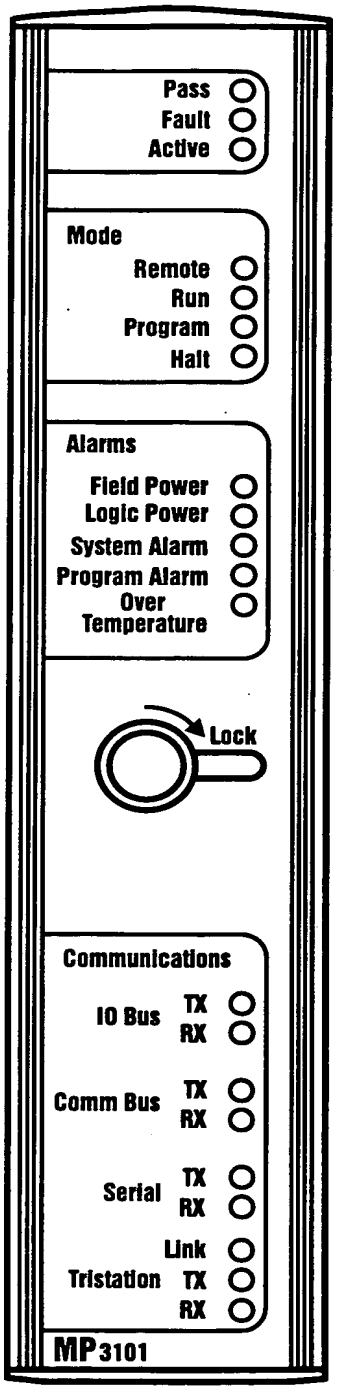

Figure 18A

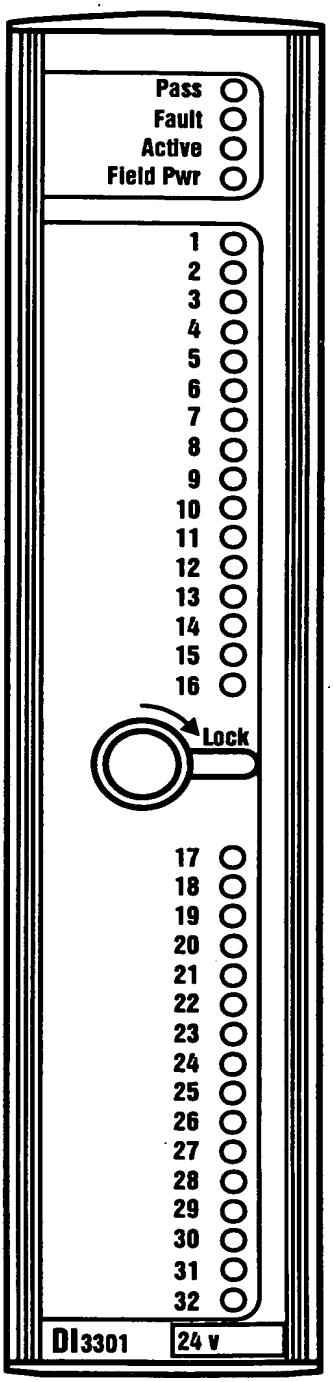

Figure 18B

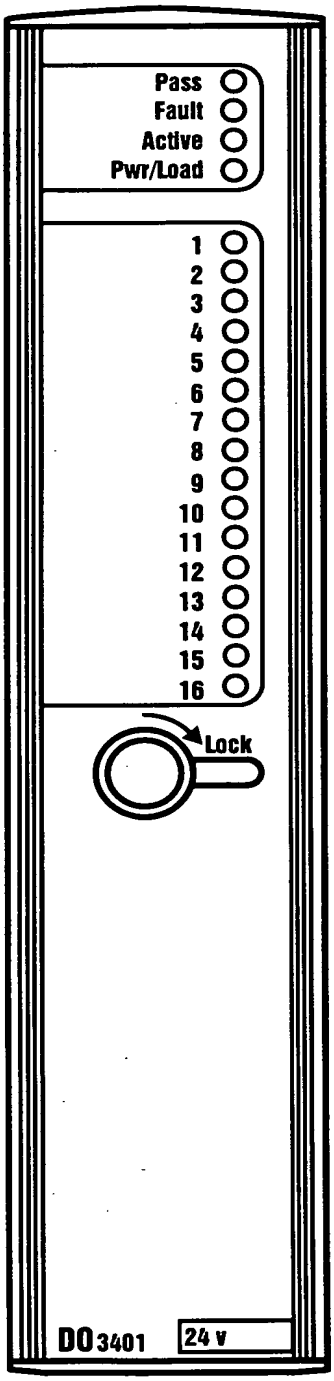

Figure 18C

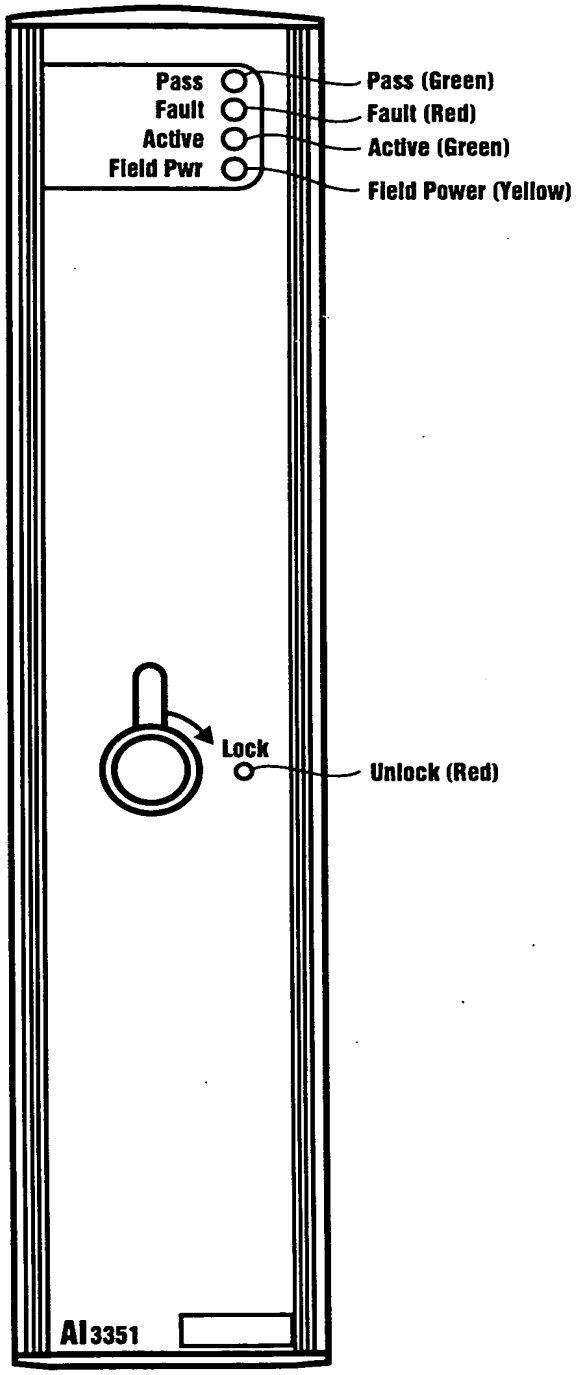

Figure 18D

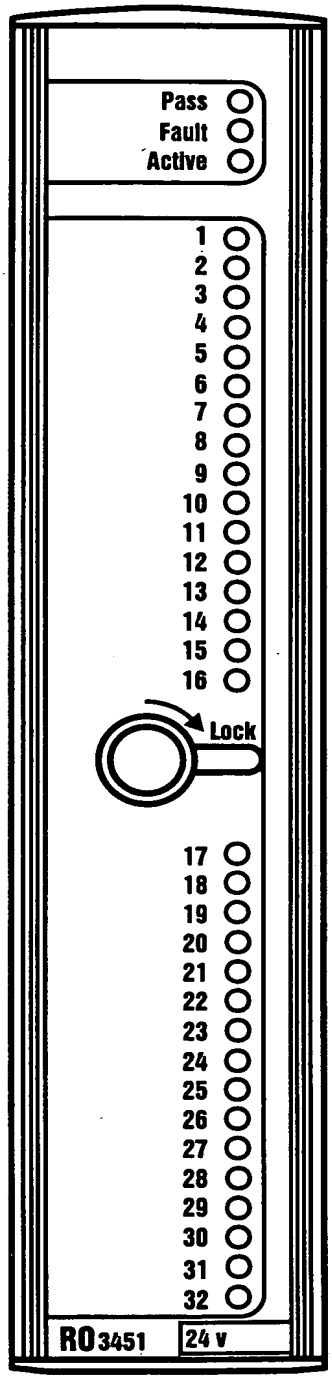

Figure 18E

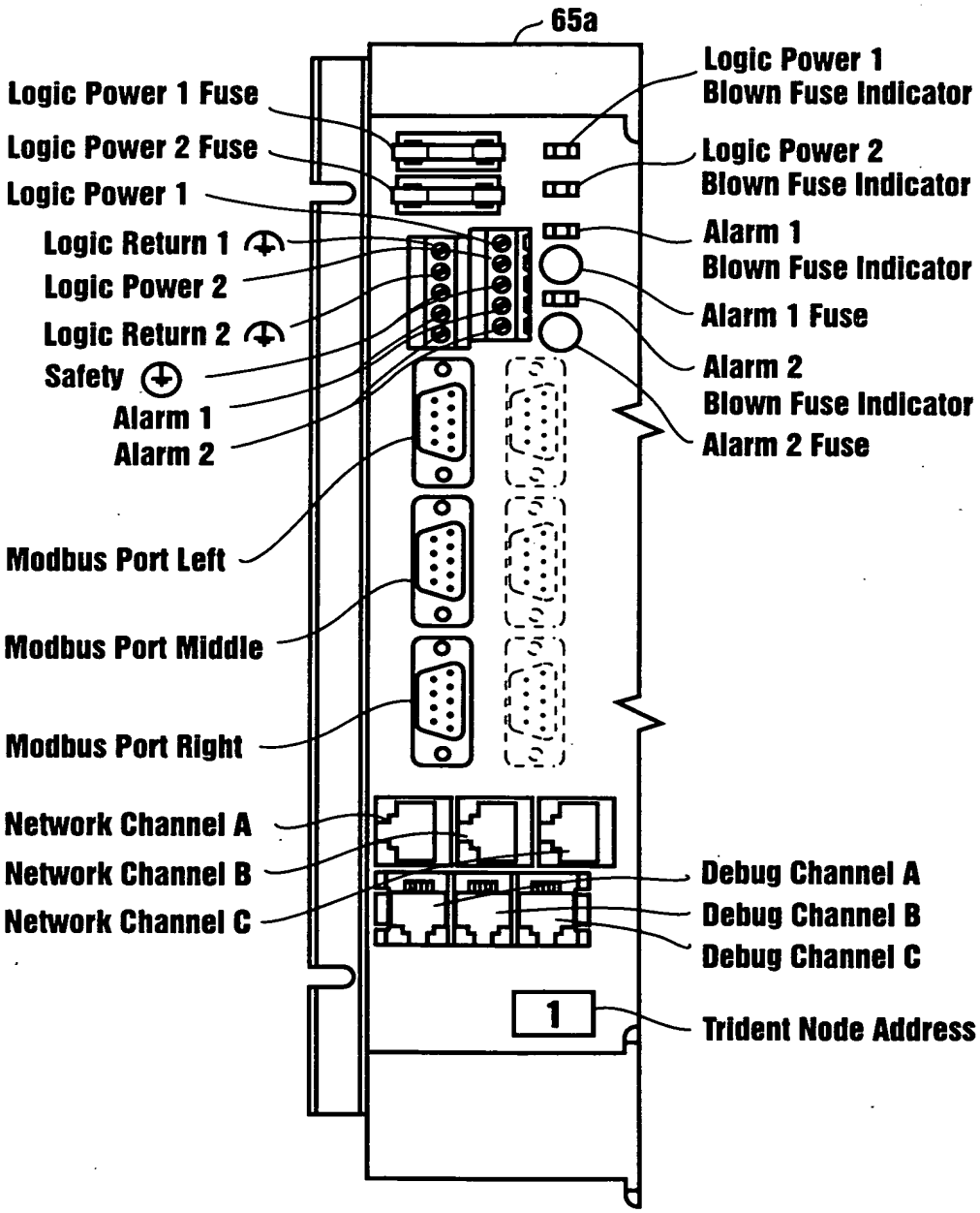
65a
Logic Power 1 Fuse
Logic Power 2 Fuse
Logic Power 1
Logic Return 1
Logic Power 2
Logic Return 2
Safety
Alarm 1
Alarm 2
Modbus Port Left
Modbus Port Middle
Modbus Port Right
Network Channel A
Network Channel B
Network Channel C
Logic Power 1 Blown Fuse Indicator
Logic Power 2 Blown Fuse Indicator
Alarm 1 Blown Fuse Indicator
Alarm 1 Fuse
Alarm 2 Blown Fuse Indicator
Alarm 2 Fuse
Debug Channel A
Debug Channel B
Debug Channel C
1
Trident Node Address

Figure 19A

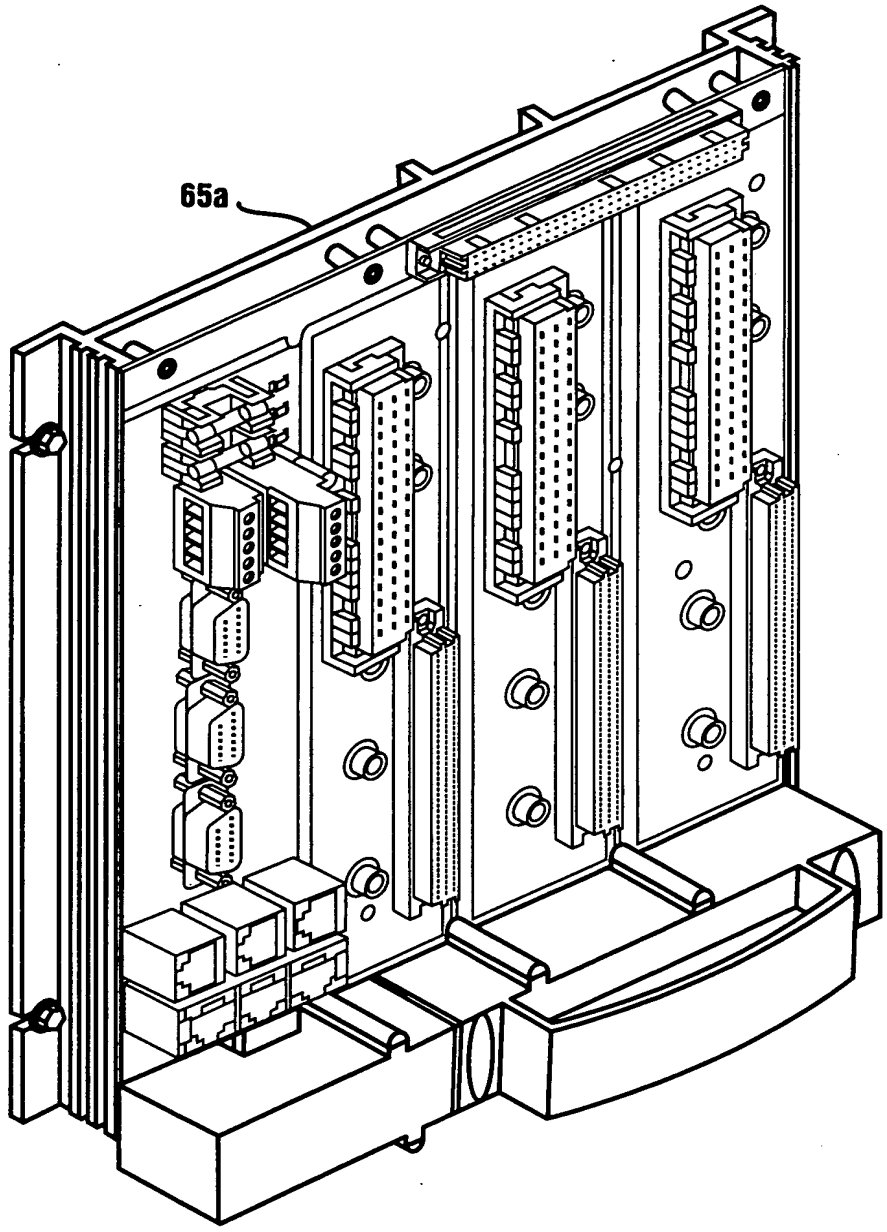

Figure 19B

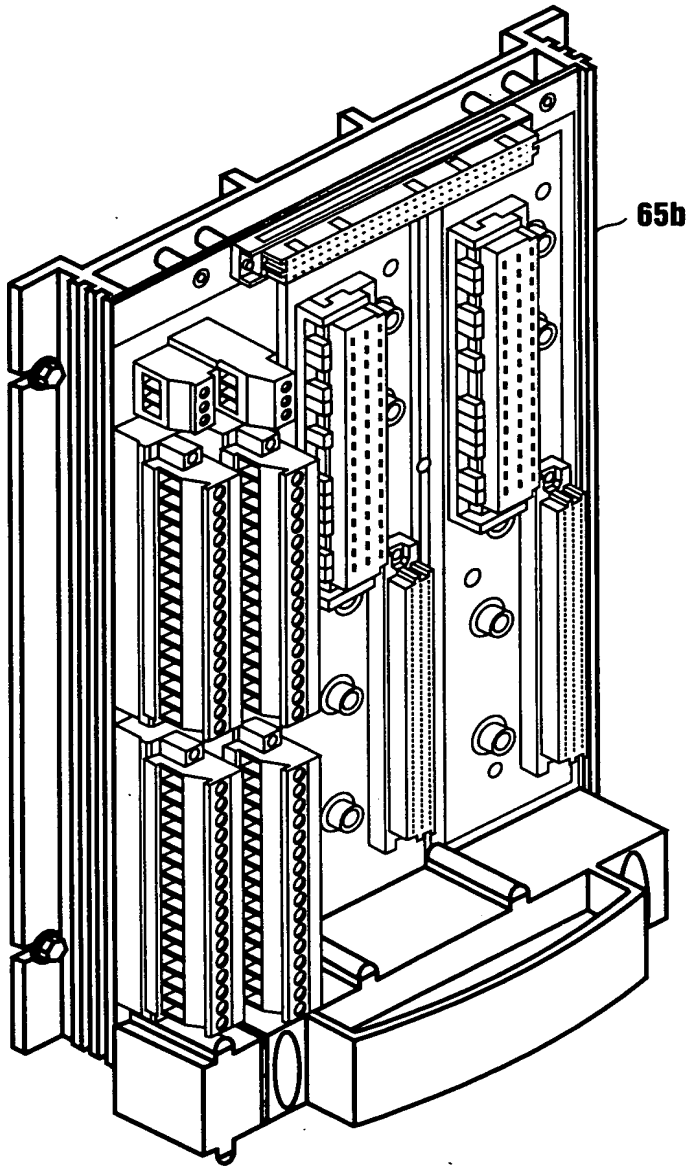

Figure 20A

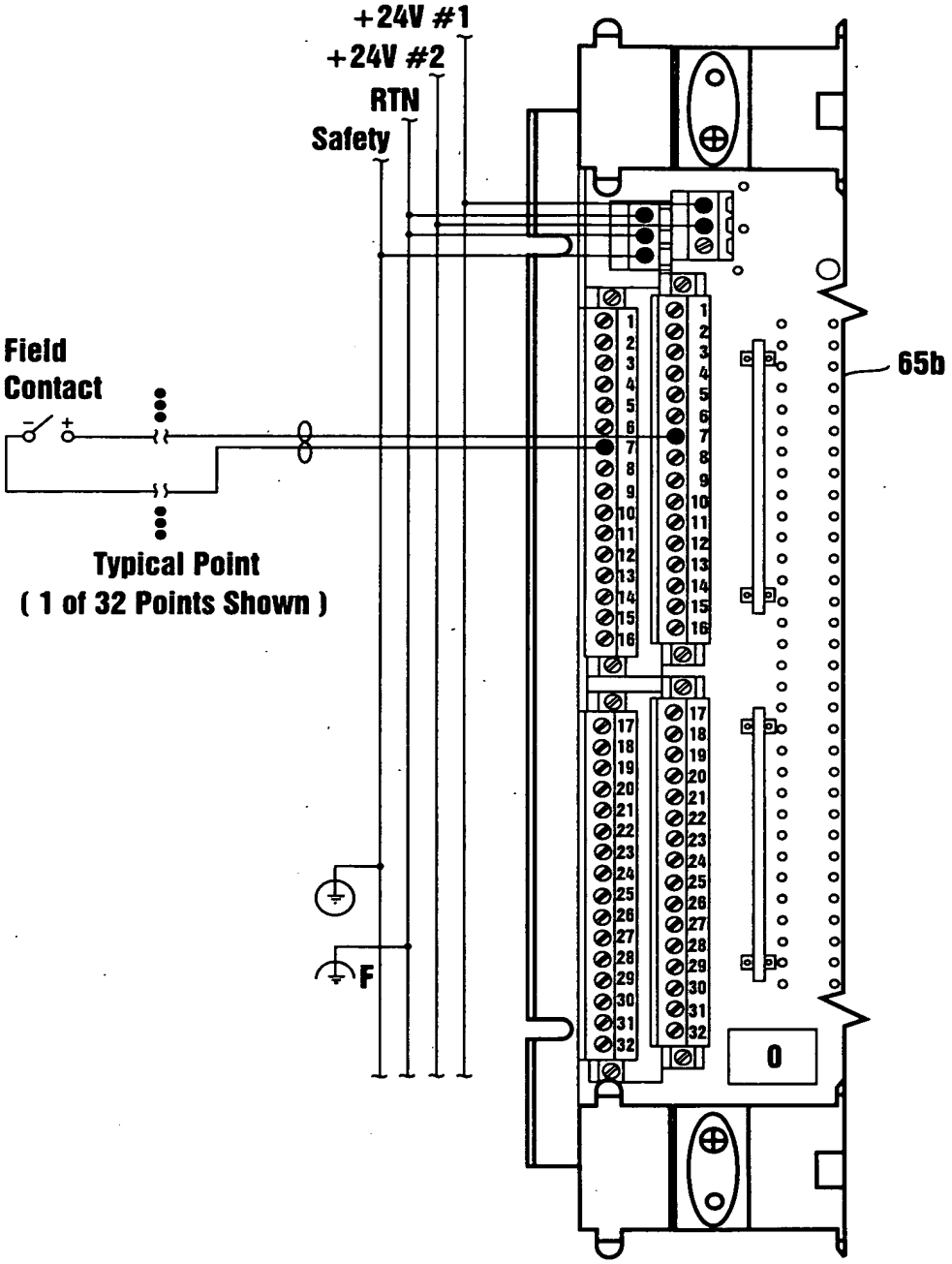
+24V #1
+24V #2
RTN
Safety
Field
Contact
Typical Point
(1 of 32 Points Shown)
F
65b
0

Figure 20B

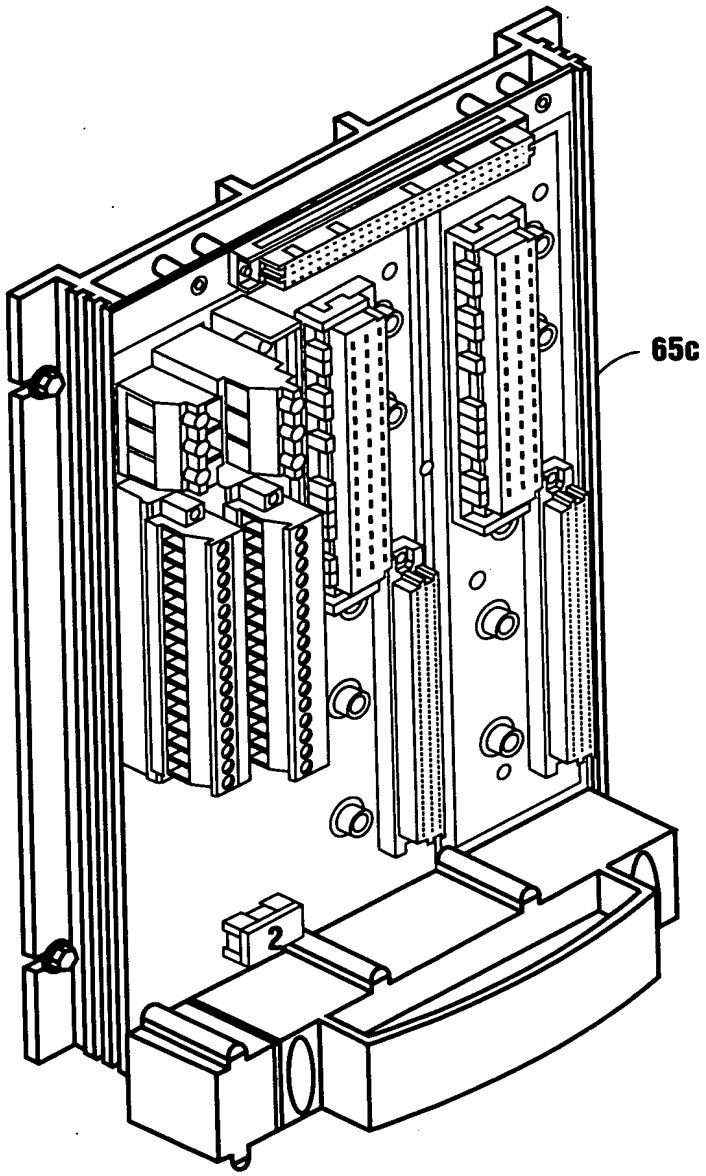

Figure 21A

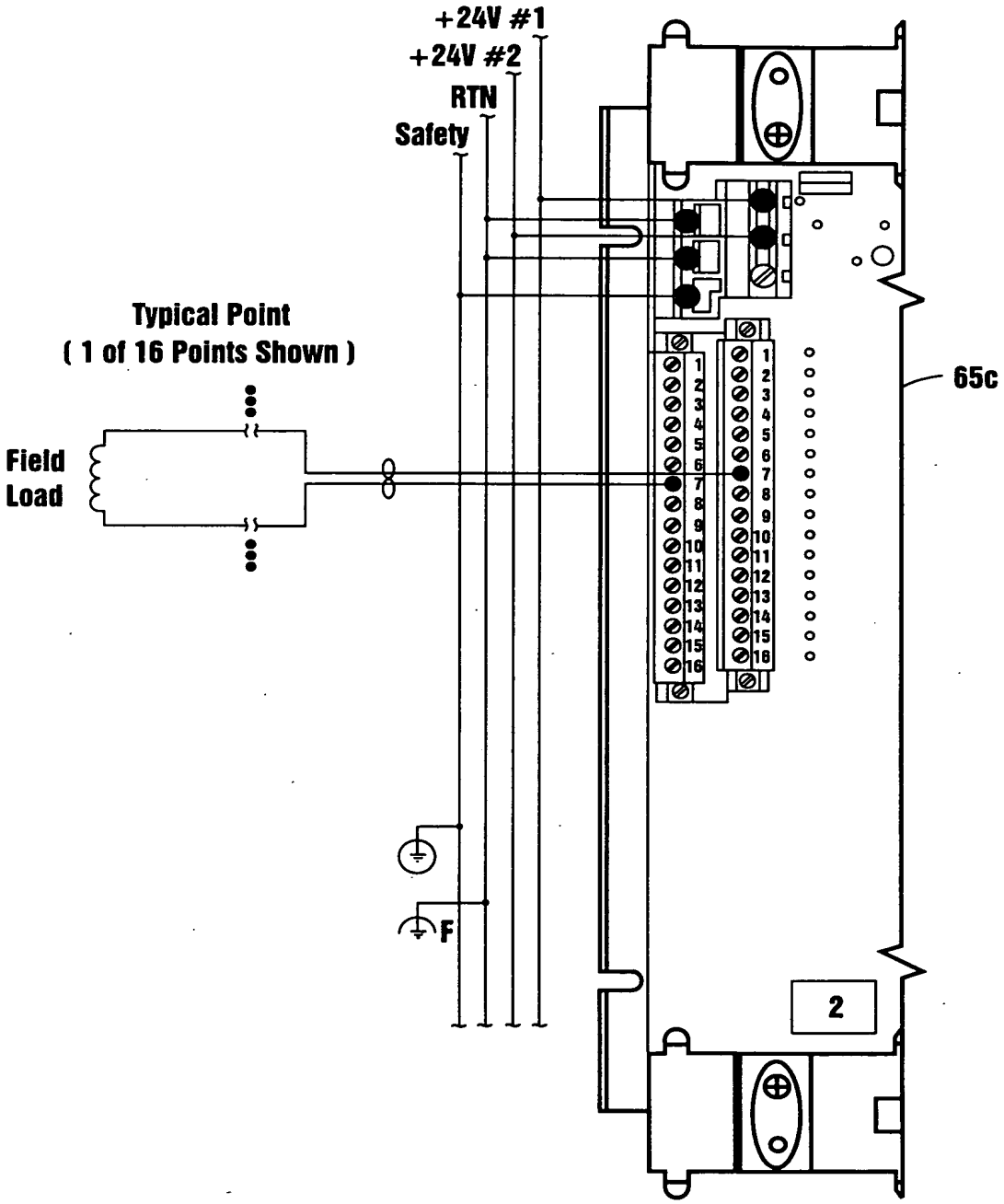
+24V #1
+24V #2
RTN
Safety
Typical Point
(1 of 16 Points Shown)
Field
Load
65c
F
2

Figure 21B

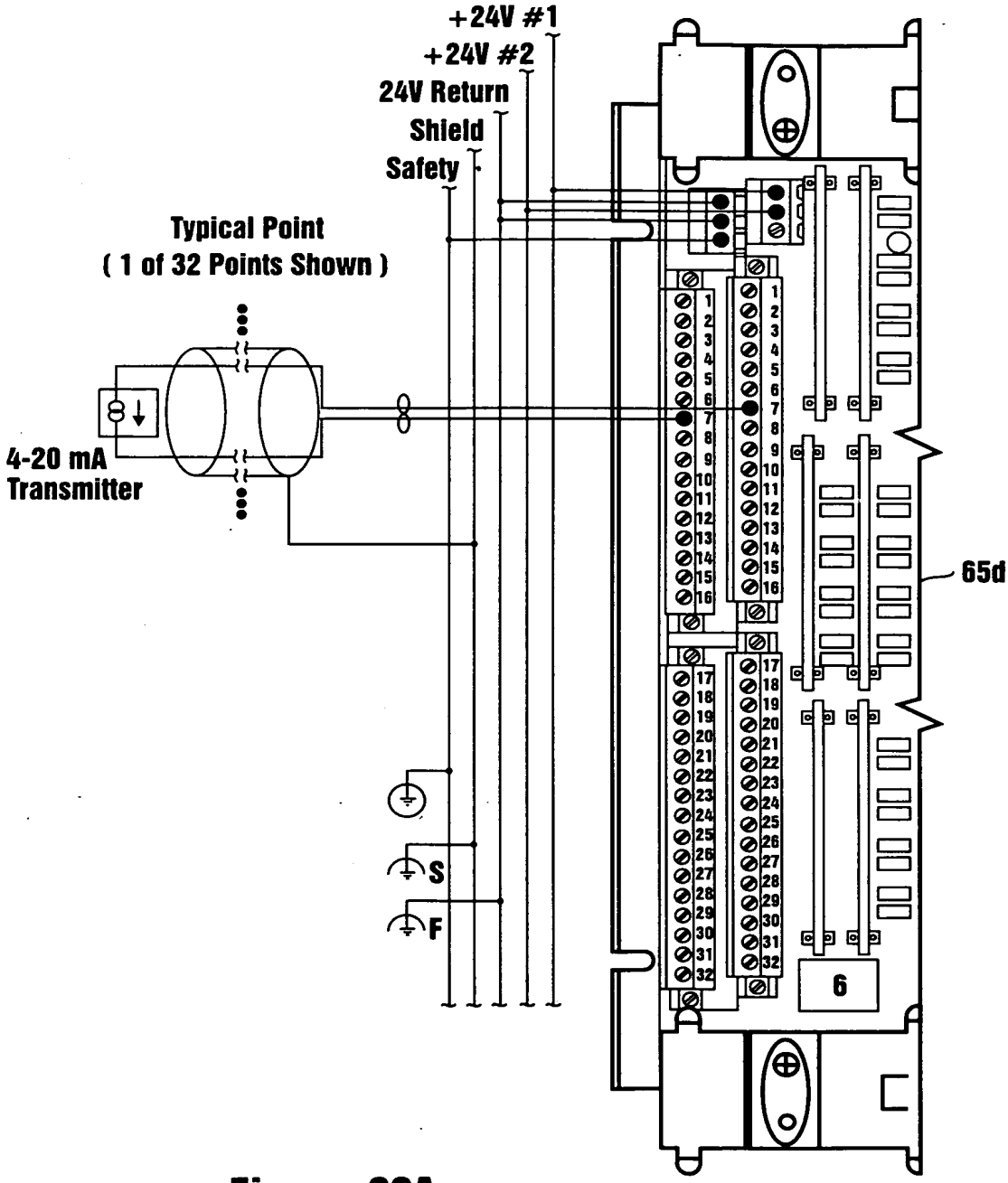
+24V #1
+24V #2
24V Return
Shield
Safety
Typical Point
(1 of 32 Points Shown)
4-20 mA
Transmitter
S
F
65d
6

Figure 22A

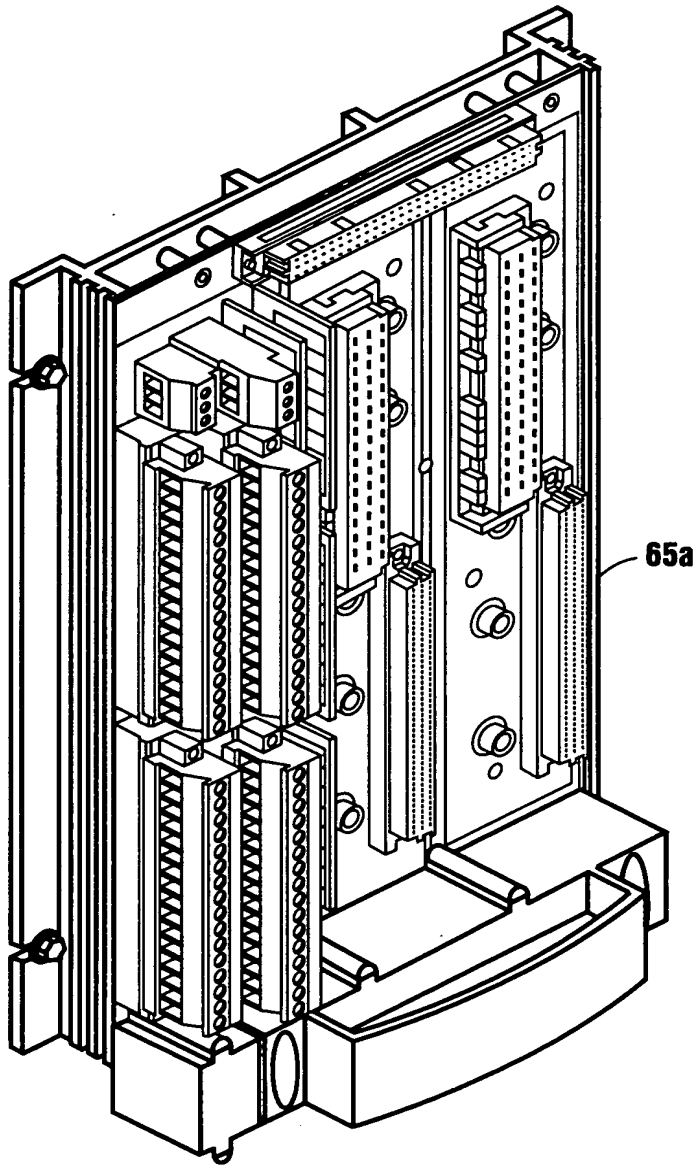

Figure 22B

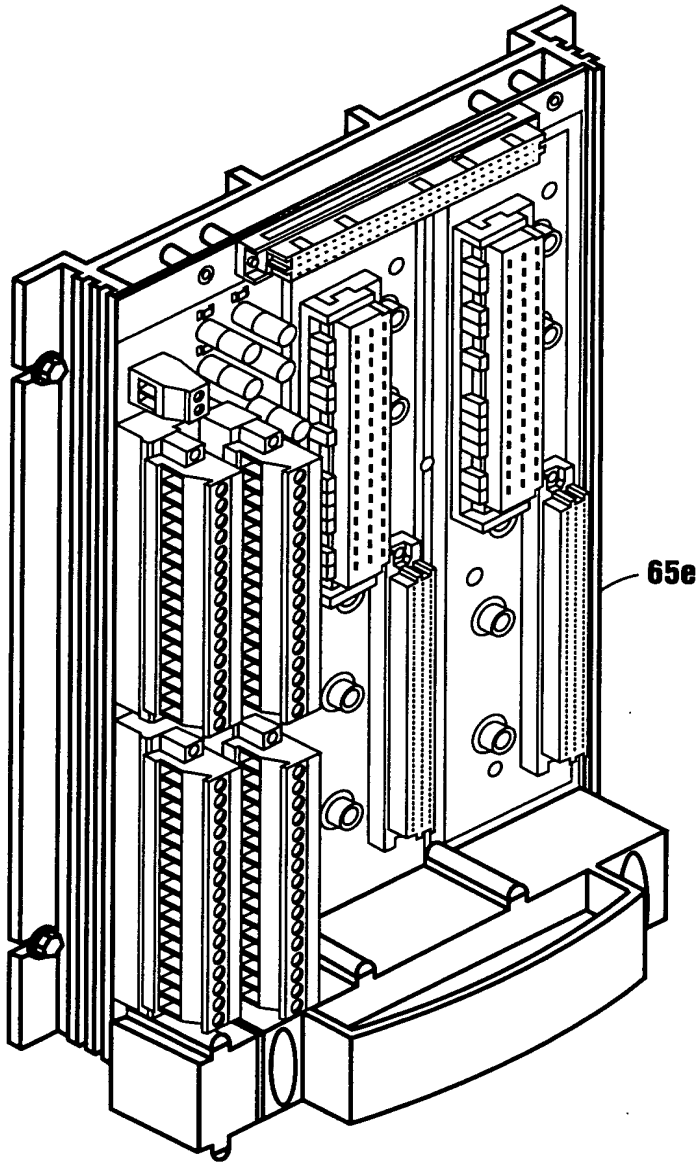

Figure 23A

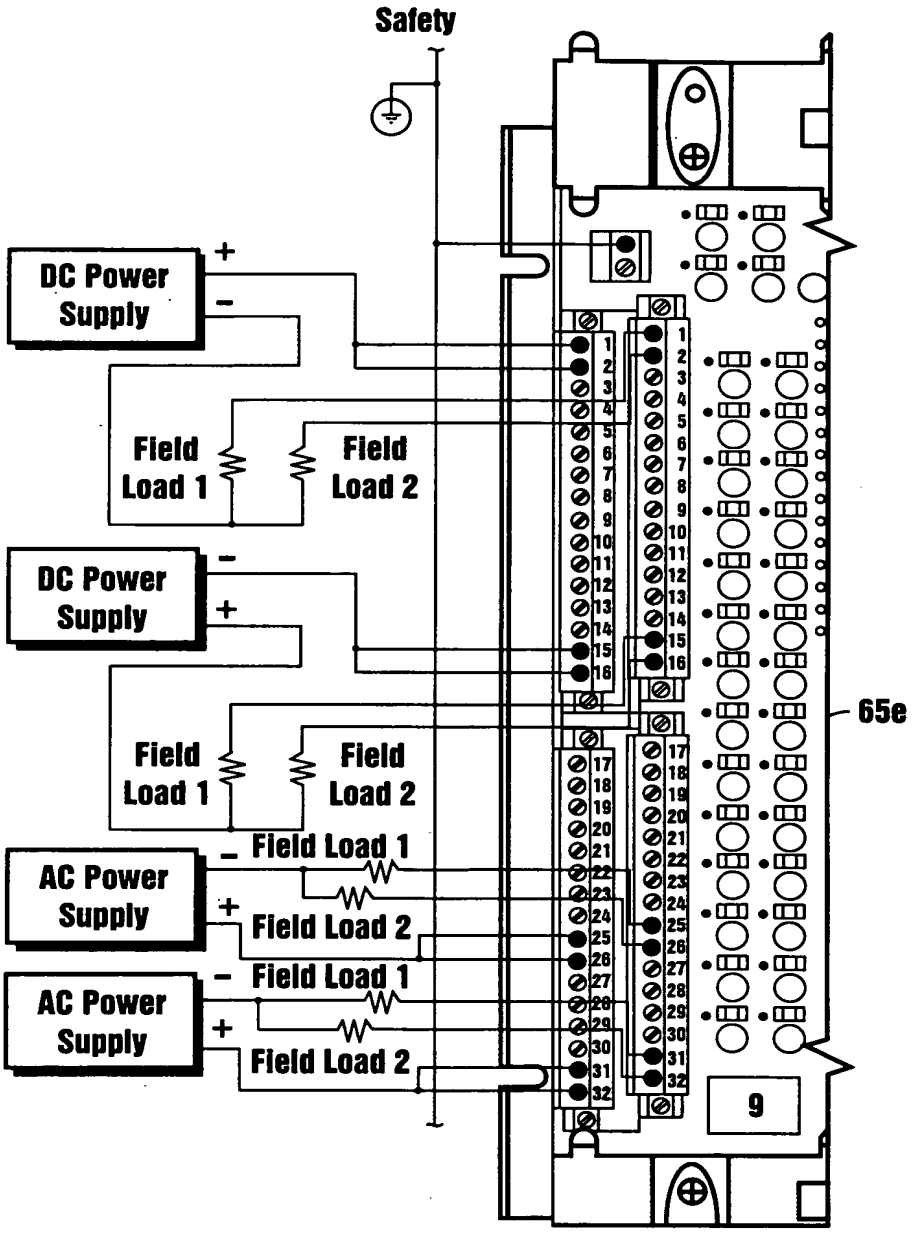
Safety
DC Power Supply
+
-
Field Load 1
Field Load 2
DC Power Supply
-
+
Field Load 1
Field Load 2
AC Power Supply
-
Field Load 1
+
Field Load 2
AC Power Supply
-
Field Load 1
+
Field Load 2
65e
9

Figure 23B

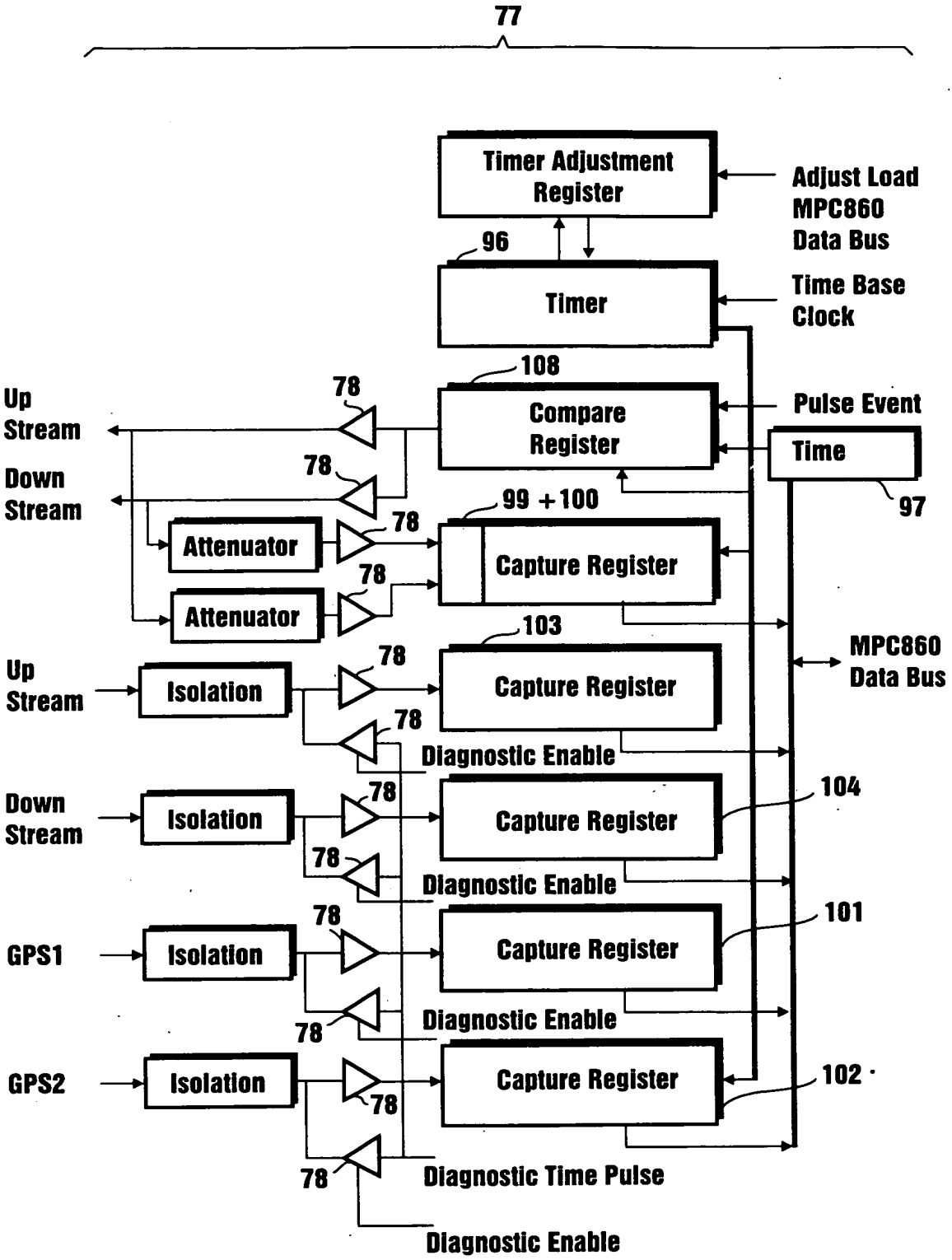
77
Timer Adjustment Register
Adjust Load MPC860 Data Bus
96
Timer
Time Base Clock
108
Compare Register
Pulse Event
Time
97
99 +100
Capture Register
Up Stream
Down Stream
Attenuator
Attenuator
78
103
Capture Register
MPC860 Data Bus
Isolation
Diagnostic Enable
104
Capture Register
GPS1
101
Capture Register
GPS2
102
Capture Register
Diagnostic Time Pulse
Diagnostic Enable

Figure 24

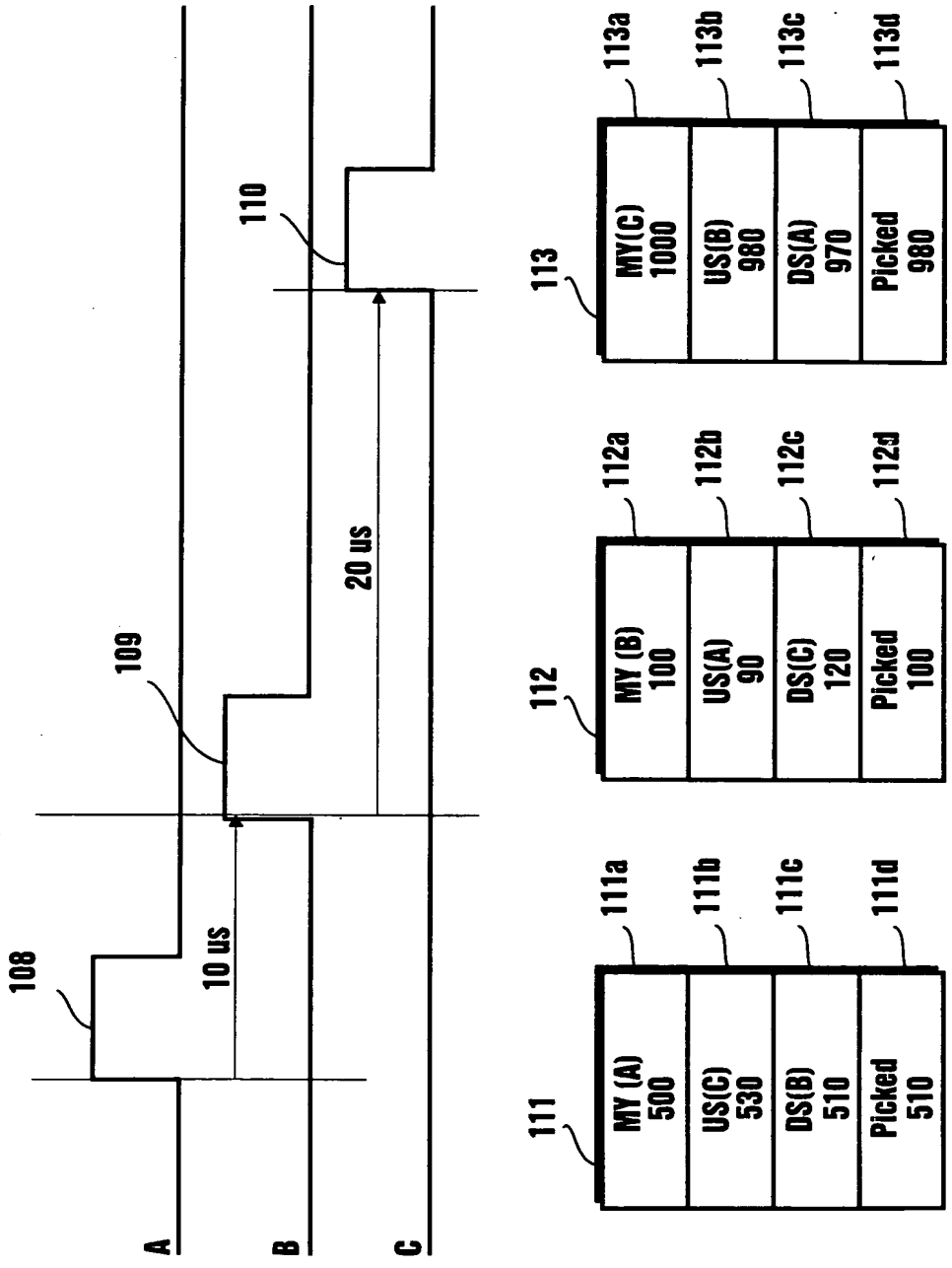
A
B
C
108
109
110
10 us
20 us
111
111a
MY (A) 500
111b
US(C) 530
111c
DS(B) 510
111d
Picked 510
112
112a
MY (B) 100
112b
US(A) 90
112c
DS(C) 120
112d
Picked 100
113
113a
MY(C) 1000
113b
US(B) 980
113c
DS(A) 970
113d
Picked 980

Figure 25